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**PCB BOARD SIZE**  
**8 Layers**  
**198mmX184mm**  
**Thickness: 1.6mm**

#### BOM Configuration

Unmount:(R\_)  
XDP:(X\_)  
OCP:(O\_)  
Q170 SKU:(Q\_)  
DP:(DP\_)  
USB\_TYPE C:(TYPEC\_)  
USB\_TYPE A:(TYPEA\_)  
3L 前掀式 SATA CONN:(SF\_)  
3L 後掀式 SATA CONN:(SB\_)

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PCB:16531  
Project Code: 3PD08F010001

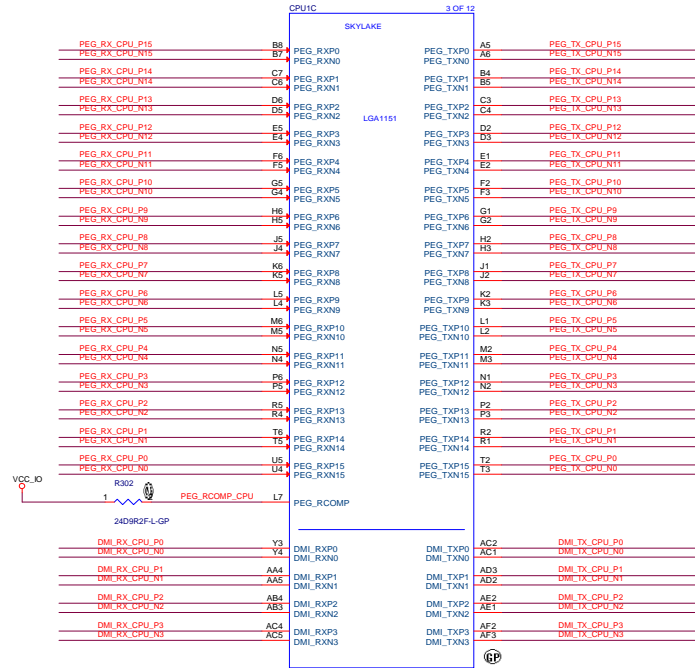


PEG

93 PEG\_TX\_CPU\_P0..15] <<<  
93 PEG\_TX\_CPU\_N0..15] <<<  
93 PEG\_RX\_CPU\_P0..15] <<<  
93 PEG\_RX\_CPU\_N0..15] <<<

DMI

16 DMI\_RX\_CPU\_P0..3] <<<  
16 DMI\_RX\_CPU\_N0..3] <<<  
16 DMI\_TX\_CPU\_P0..3] <<<  
16 DMI\_TX\_CPU\_N0..3] <<<



## CPU XDP

H\_TDO  
H\_TDI  
H\_TMS  
H\_TCK

H\_TRST\_N  
H\_PREQ\_N  
H\_PROG\_N

## SVID

VIDSCK\_VR1      >>—

VIDSOUT\_VR1      >>—

VIDALERT#\_VR1      >>—

CLOCK

CPU\_BCLK\_PCH  
CPU\_BCLK\_PCH#

CPU\_P0BCLK\_PCH  
CPU\_P0BCLK\_PCH#

CPU\_CLK24M\_PCH  
CPU\_CLK24M\_PCH#

## CONTROL

4,46	PROCHOTR_R	»»
51	DOR_VTT_CNTL	»»
	CPU_VCCST_PWRGD	»»
0,65	H_PWRGD	»»
15	PLTRST_CPU_N	»»
7	PM_SYNC_CPU	»»
7	PM_DOWN_PCH	««
24	PECI_CPU	««
	THERMTRIP#_CPU_R	««
16	H_SKTOCC_N	««

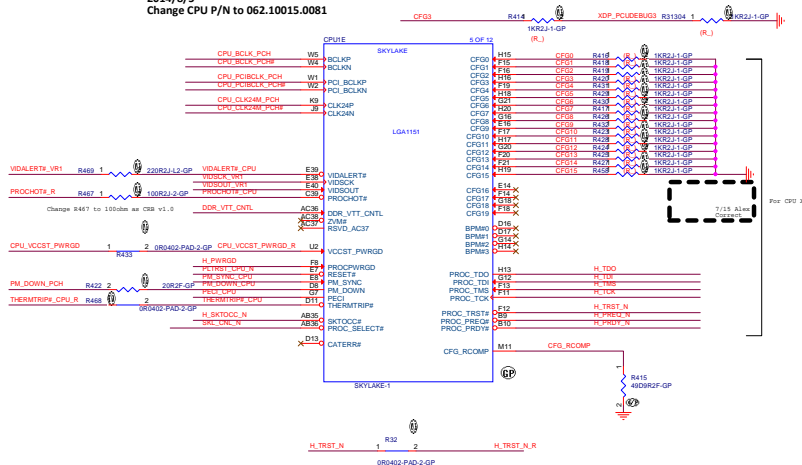
PCH\_JTAG\_TDO  
PCH\_JTAG\_TDI  
PCH\_JTAG\_TMS  
H\_TRST\_N\_R

VIDSCK  
VIDSOUT  
VIDALERT#  
Need to add Pull UP on both CPU and VR side.

Signal	W1 [inches]	W2 [inches]	W3/4/ 5 [inches]	W2+W3+W4+W 5 [inches]	W51 [inches]	W52 [inches]	R <sub>W01</sub> [Ω]	R <sub>W02</sub> [Ω]	R <sub>2</sub> [Ω]	R <sub>22</sub> [Ω]	V <sub>0</sub> [V]
VID50K	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1
VID50K					Empty			45	0	50	
VIDALERT #							56	Empty	220	0	

[illegible]

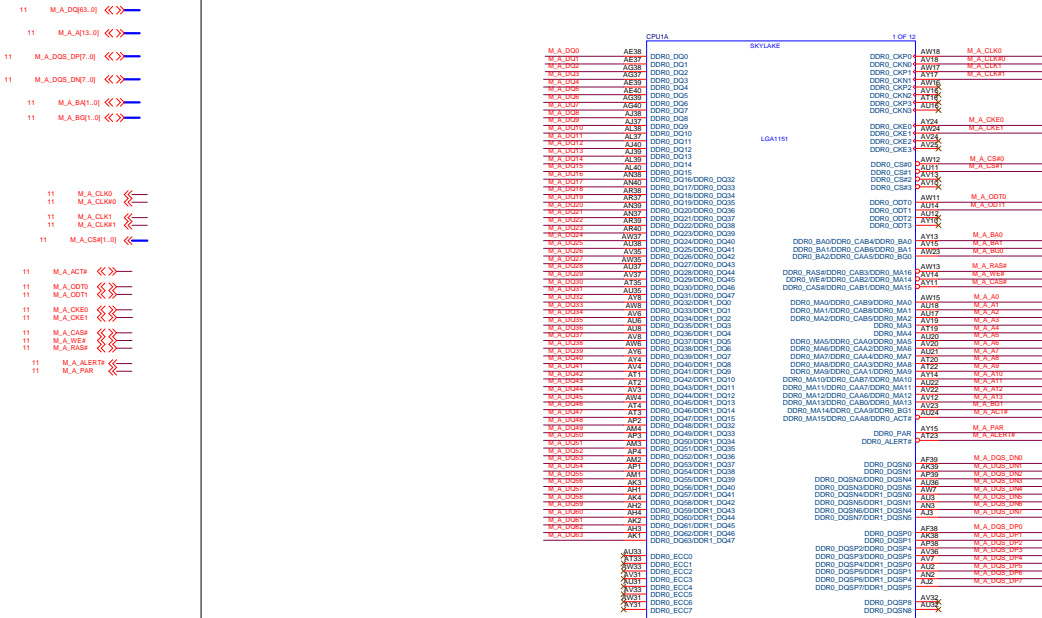
2014/8/5  
Change CPU P/N to 062.10015.0081



- **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted:
  - 1 = (Default) Normal Operation;
  - 0 = Stall.
- **CFG[1]:** Reserved configuration lane.
- **CFG[2]:** PCI Express\* Static x16 Lane Numbering Reversal:
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- **CFG[3]:** Reserved configuration lane.
- **CFG[4]:** PCIe enable:
  - 1 = Disabled.
  - 0 = Enabled.
- **CFG[6:5]:** PCI Express\* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express\*
  - 01 = reserved
  - 10 = 2 x8 PCI Express\*
  - 11 = 1 x16 PCI Express\*
- **CFG[7]:** PEG Train
  - 1 = (default) PEG Train immediately following RESET# de assertion.
  - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]:** Reserved configuration lanes.

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<b>CPU_THERMAL/CLOCK/PM/CFG</b>	
Title	Rev
Size Custom	Document Number <b>Iroxbox2</b> Rev <b>-1</b>
Date November 28th 2017	ESD 4 of 120





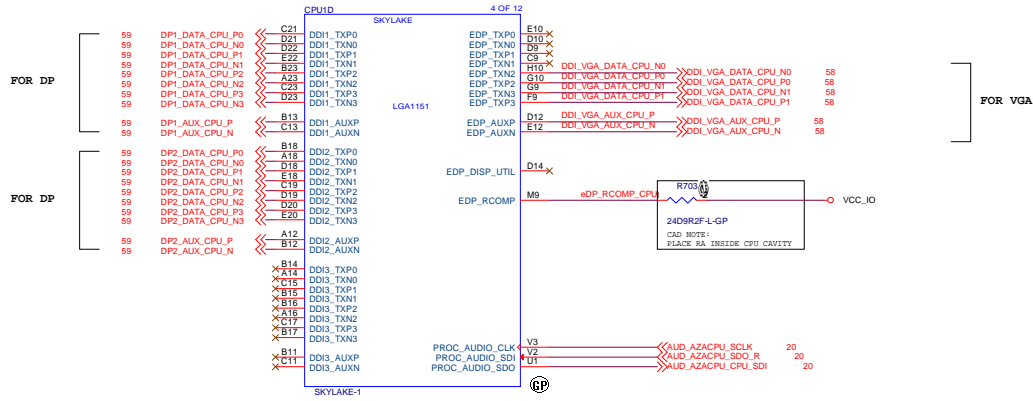


2014/8/5  
Change CPU P/N to 062.10015.0081

VBIOS set as DP

**Note:**

- When using eDP bifurcation:
  - x2 eDP lanes for eDP panel (eDP\_TXP[0:1], eDP\_TXN[0:1])
  - x2 lanes for DP (eDP\_TXP[2:3], eDP\_TXN[2:3])



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**Wistron Incorporated**  
21F, 88, Sec.1, Hsin Tai Wu Rd  
Hsichih, Taipei Hsien

**CPU (D0VEDP)**

**iroxbox2**

Date: Thursday, March 02, 2017

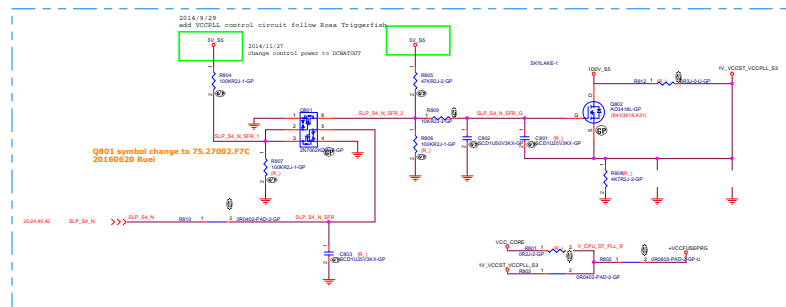
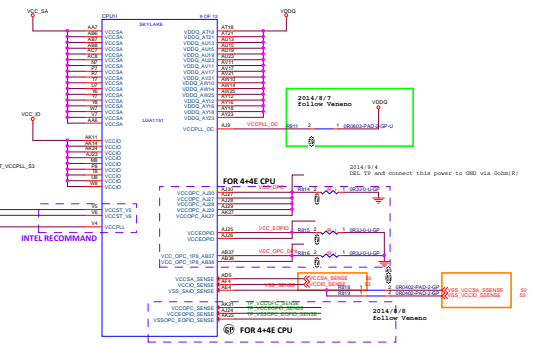
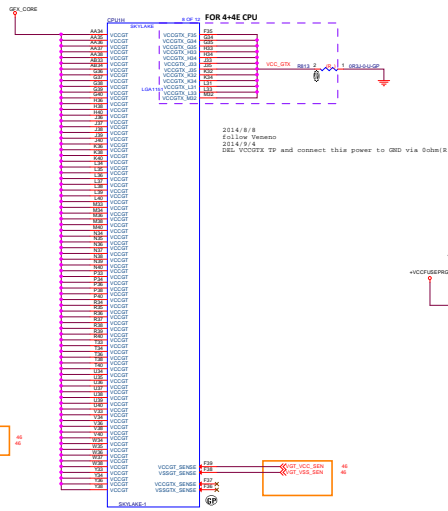
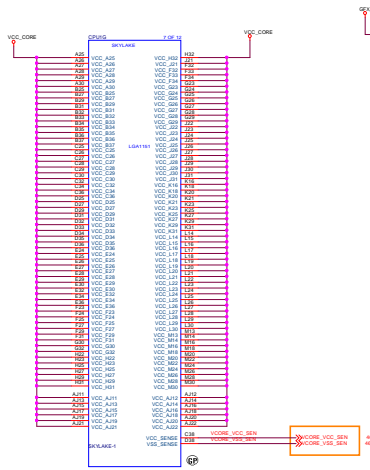
Sheet 7 of 107

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## Greenlow Server Reference Circuit: Unused Power Pins Handling

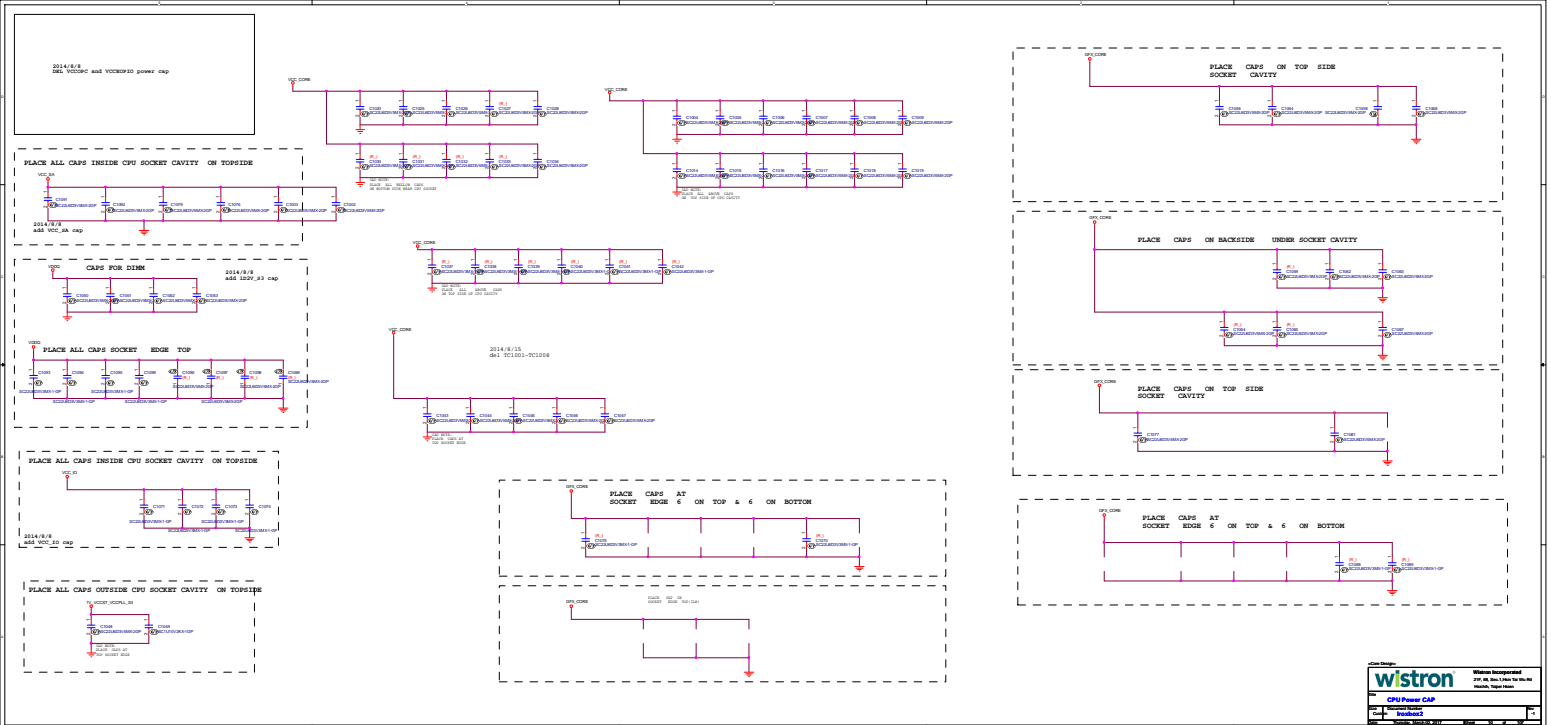
Greenlow Server Reference board Zumba Beach does not support pGFX and EDRAM, hence some of the power rails such as VCCGT, VCCGT\_X, VCC\_OPC, 1P8, VCCOCP and VCCOPIO are not required to be powered. Customers are recommended to reserve a 0 OHM 1/10W resistor between each power rail and GND. This provides the flexibility for the case where the validation results indicate the signals are good to be tied to GND or leave as unconnected. The final connection of these unused power rails will be updated in the Greenlow Server Platform Design Guide Rev 1.0 (IBP #541284, currently still at revision 0.75). Revision 1.0 is planned to be released around WW43.

2014/8/5  
Change CPU P/N to 062.10015.0081



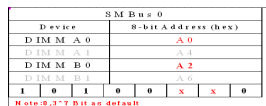
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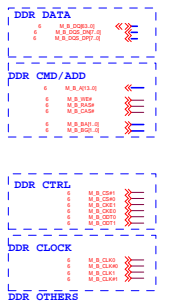




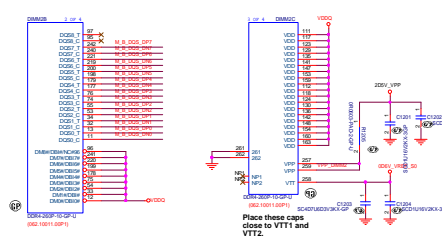
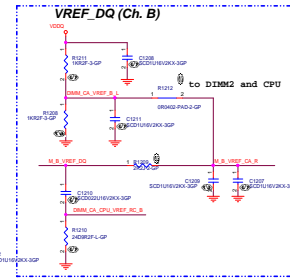
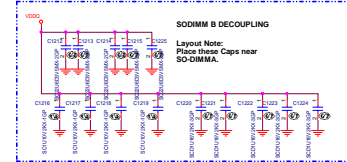
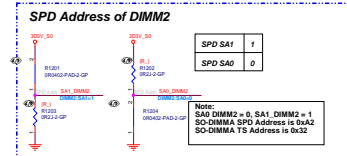
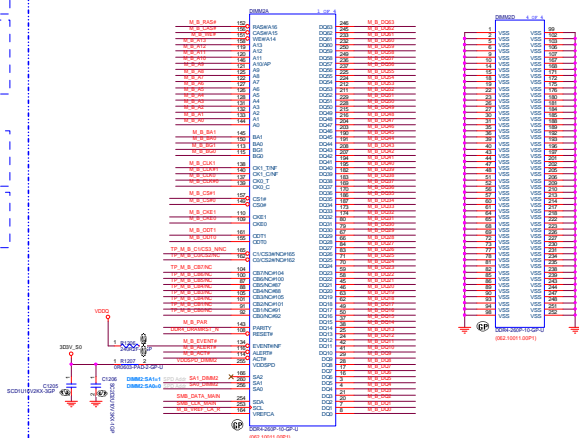
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# CHANNEL-B DIMM2, A2, H=4mm



SMBus 0	
Device	8-bit Address (hex)
DIMM A 0	A 0
DIMM B 0	A 2
DIMM B 1	A 0
1 0 1 0 1 0 0 0	x x 0

Note: 0-7 bit is default

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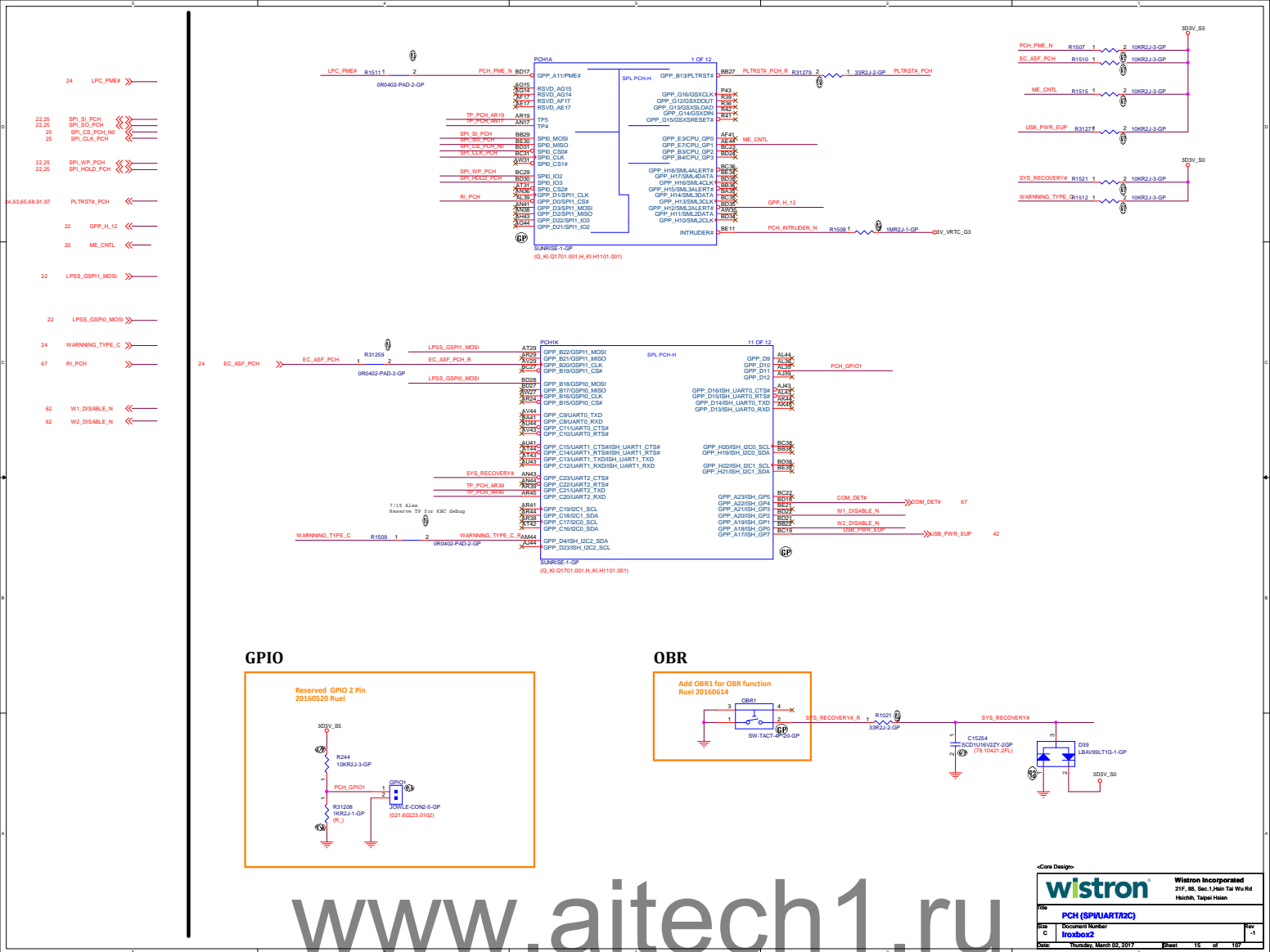
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Title					
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Date	Thursday, March 09, 2017		Sheet 14 of 107

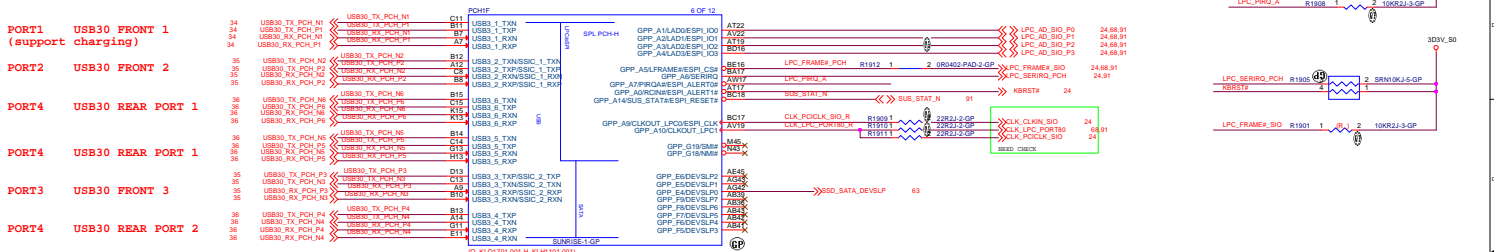
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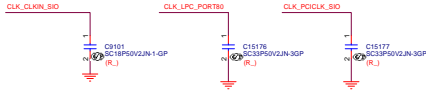




Integrated Pull-ups and Pull-downs

Signal	Resistor Type	Value	Notes
LAD[3:0]	Pull-up	15 ~ 40 kΩ	

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB3.0	USB3.0	USB3.0	USB3.0	N/A	N/A	N/A	N/A	N/A	N/A	LAN	LAN	PCle	PCle
G150	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	N/A	N/A	LAN	LAN	PCle	PCle
H170	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	LAN	LAN	PCle	PCle
C170	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	LAN	LAN	PCle	PCle



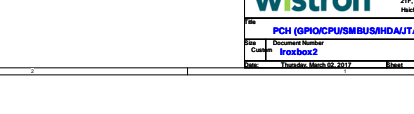
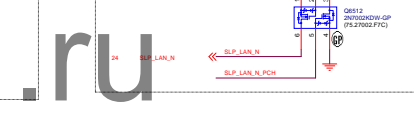
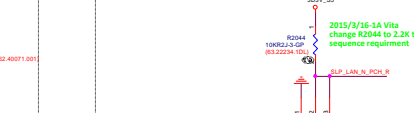
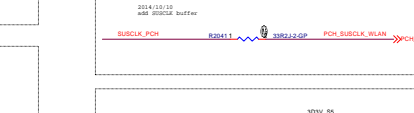
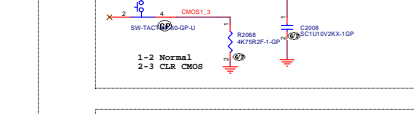
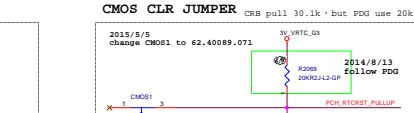
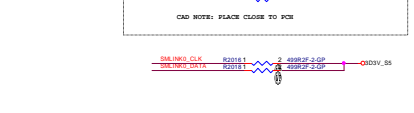
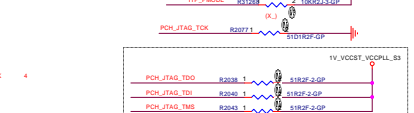
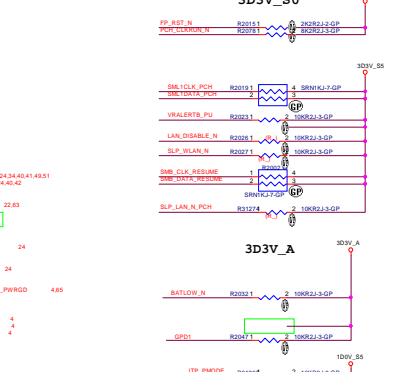
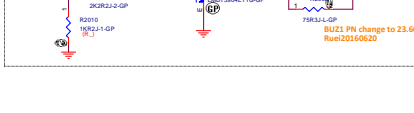
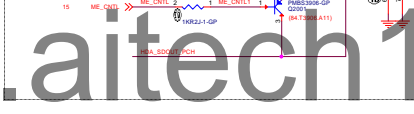
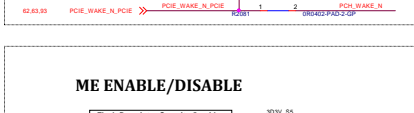
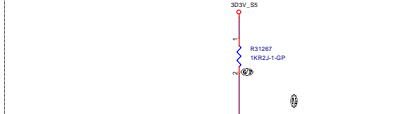
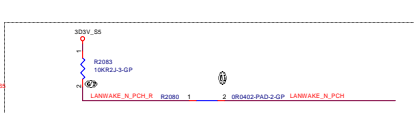
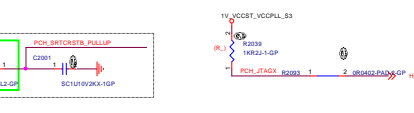
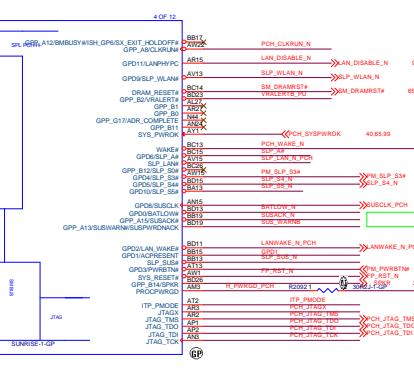
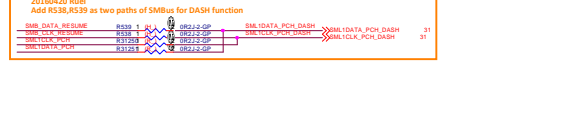
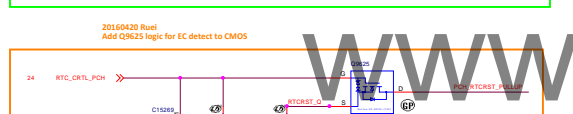
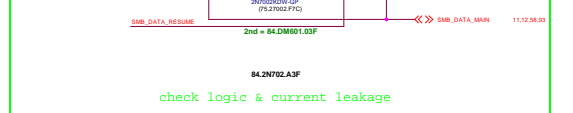
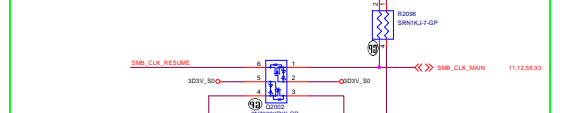
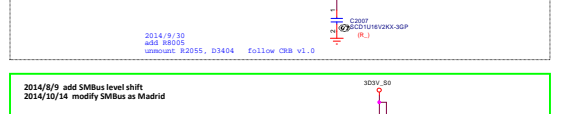
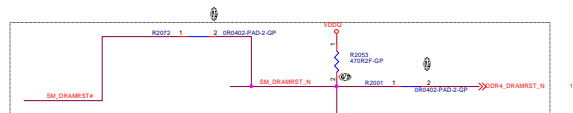
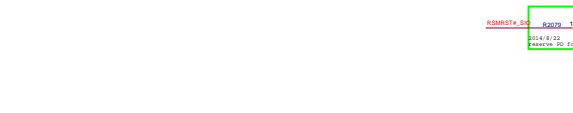
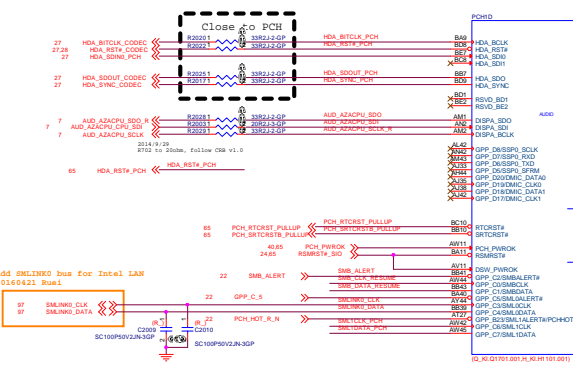
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PCH (USB/ESPI)  
Rev  
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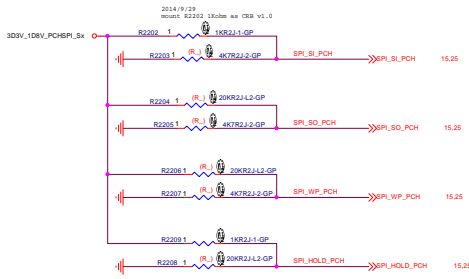
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Iracor2  
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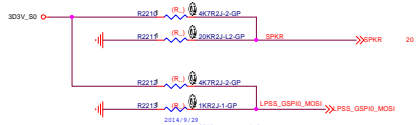




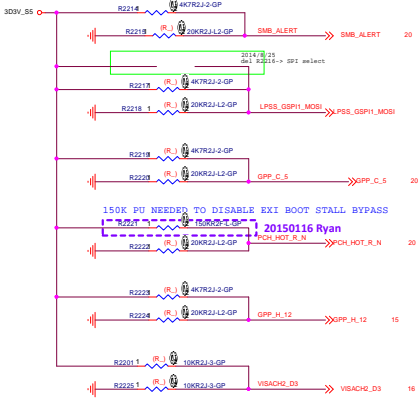
# PCH STRAP FUNCTIONS



SPI_SI_PCH (SPI0_MOSI)	0: Enable boot halt 1: Disable boot halt The internal PU resistor is enabled when RSMRST# is asserted and is switched to the internal PD when RSMRST# is de-asserted.
SPI_SO_PCH (SPI0_MISO)	0: Disable JTAG ODT 1: Enable JTAG ODT The internal PU resistor is enabled when RSMRST# is asserted
SPI_WP_PCH (SPI0_IO2)	0: Enable consent strap 1: Disable consent strap PCH has internal weak PU
SPI_HOLD_PCH (SPI0_IO3)	0: Enable personality strap 1: Disable personality strap PCH has internal weak PU



SPKR (SPKR / GPP_B14)	0: Disable Top Swap mode. (Default) 1: Enable Top Swap mode. PCH internal pull-down is disabled after PLTRST# deasserts.
LPSS_GSPH_MOSI (GPP_B18/GSPH0_MOSI)	0: Disable No Reboot mode. 1: Enable No Reboot mode This function is useful when running ITR/SDP. The internal pull-down is disabled after PLTRST# deasserts.
PCH_PORT80_LED (GPP_C2/SMBALERT#)	0: Disable TSL confidentiality 1: Enable TSL confidentiality (default) The internal pull-down is disabled after RSMRST# deasserts.
LPSS_GSPI1_MOSI (GPP_B22/GSPI1_MOSI)	BOOT SELECT STRAP 0: SPI select 1: LPC select The internal pull-down is disabled after PLTRST# deasserts.



GPP_C_5 (GPP_C5/SML0ALERT#)	ESP1/EC - SELECT - STRAP 0: LPC is selected for EC. 1: eSPI is selected for EC. The internal pull-down is disabled after RSMRST# deasserts.
PCH_HOT_R_N (GPP_B23/SML1ALERT#/PCHHOT#)	0: Disable Exi boot stall bypass 1: Enable Exi boot stall bypass The internal PD resistor is disabled after RSMRST# de-asserted.
GPP_H_12 (GPP_H12/SML2ALERT#)	ESPI flash sharing mode 0: Master attached flash sharing 1: Slave attached flash sharing PCH has internal weak PD.
VISACH2_D3 (GPP_E12)	DFX test mode 0: XTAL input is single ended. 1: XTAL input is differential. The internal PD resistor is disabled after RSMRST# de-asserts
HDA_SDOUT_PCH (HDA_SDO)	0: Enable security measures defined in the Flash Descriptor. 1: Disable Flash Descriptor Security (override). The internal pull-down is disabled after PLTRST# deasserts.
SUSCLK_PCH (GPD8/SUSCLK)	0: Disable OD PLL VR 1: Enable OD PLL VR

Follow ROSA / D7 triggerfish & Lily / M800 skylake project.



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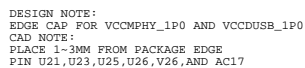
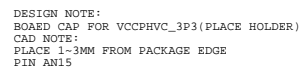
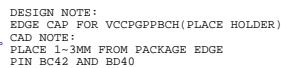
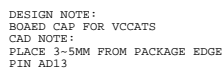
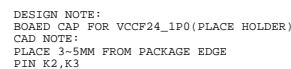
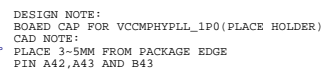
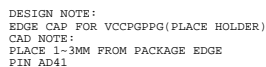
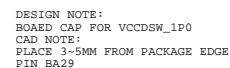
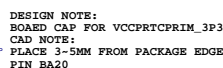
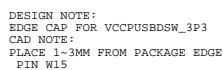
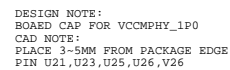
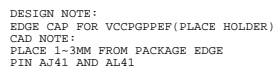
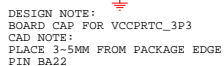
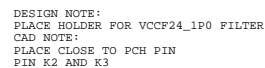
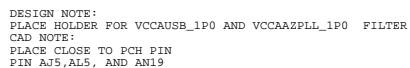
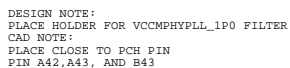
Core Design:

**wistron** Wistron Incorporated  
21F, 8B, Sec.1, Hsin Tai Wu Rd.  
Hsinchu, Taipei, Taiwan

File: **PCH (POWER2)**

Rev: **C** Document Number: **iroxbox2** Rev: **-1**

Date: **Monday, March 20, 2017** Sheet: **25** of **107**





**SPI  
ROM**

2014/8/6  
add SPI1 62.10076.011

Single Flash Device: 15ohm  
Dual Flash Device: 33ohm

### SKL Platforms – SPI0\_IO3 Signal Implementation Requirement for ES or pre-ES1/ES1 Samples

An Intel internal debug strap is implemented on the SPI0\_IO3 signal. However, the strap is not functioning as expected on ES (SKL U/Y platform) and pre-ES1/ES1 (SKL S/H platform) samples and could prevent the system from booting. The issue will be fixed in future samples.

To ensure the platform boots with these early samples, Intel recommends customers to implement a pull-down resistor on the SPI0\_IO3 signal aside from the 1 kOhm pull-up resistor which is already a requirement on the signal. There are two options to implement the pull-down resistor:

**Option 1:** Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

Option 2: Implement a strong pull-down resistor (e.g. 100 Ohm) on the signal and disable it after RSMRST# de-assertion.

Note that the pull down resistor on SPI0\_IO3 is only needed for SKL U/Y platforms with ES and SKL S/H platforms with pre-ES1/ES1 samples.

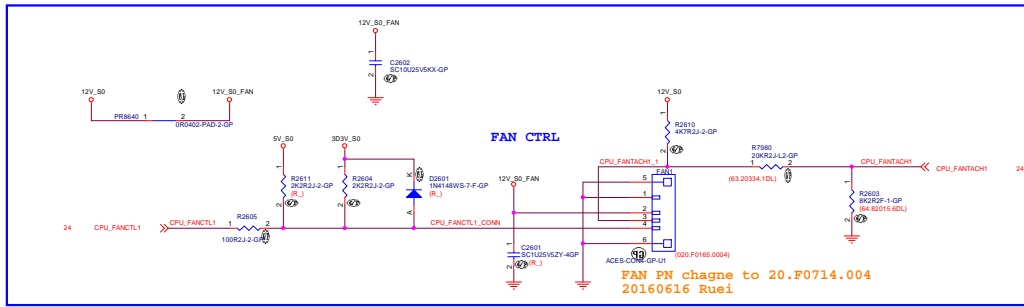


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Battery Socket
ST: 22.70017.051
FLAT: 22.70017.061

Battery (CR2032):
23.22063.001
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RTC1 PN change to 20.F2316.002  
Ruei20161013

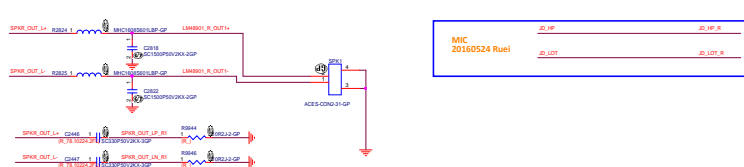
FAN design follow Hangzhou  
20160623 Ruei



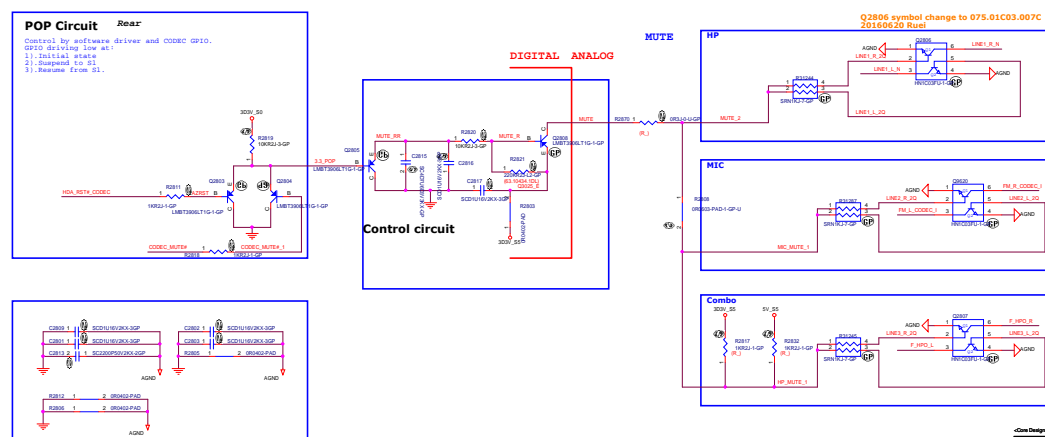
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Size	Document Number	Rev	
Custom	Ironbox2	-1	
Date	Thursday, March 02, 2017	Sheet	26 of 187

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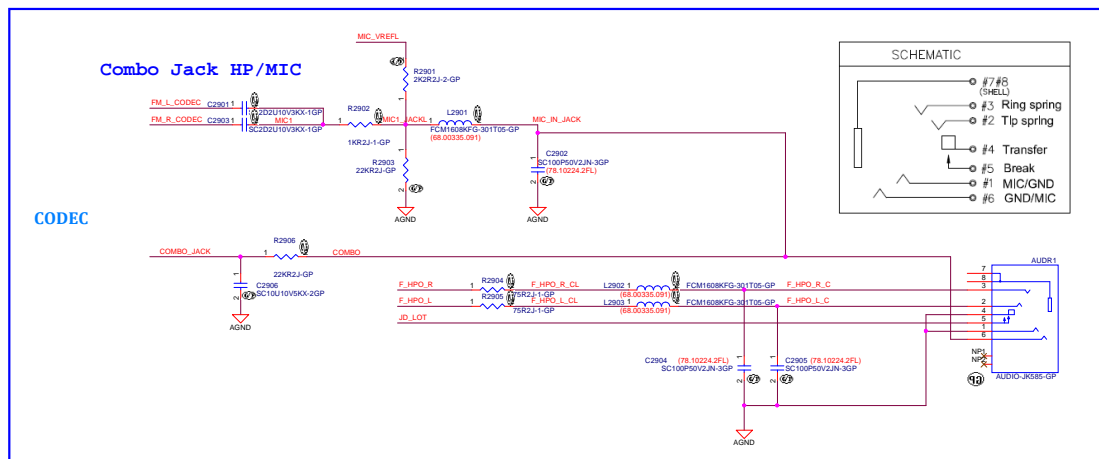
SPK1 Pn change to 20.F1606.002  
20160616 Ruei



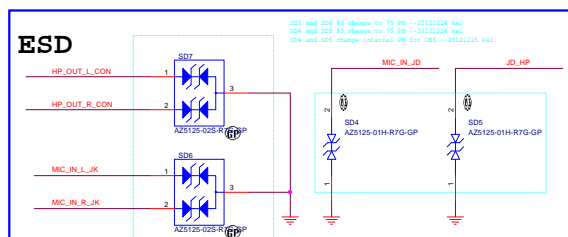
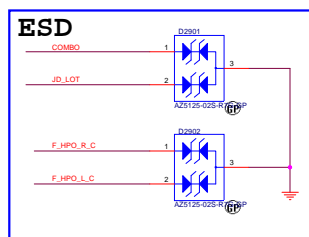
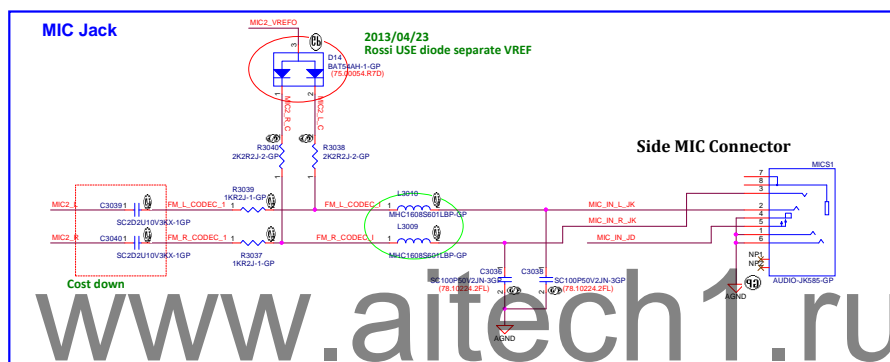
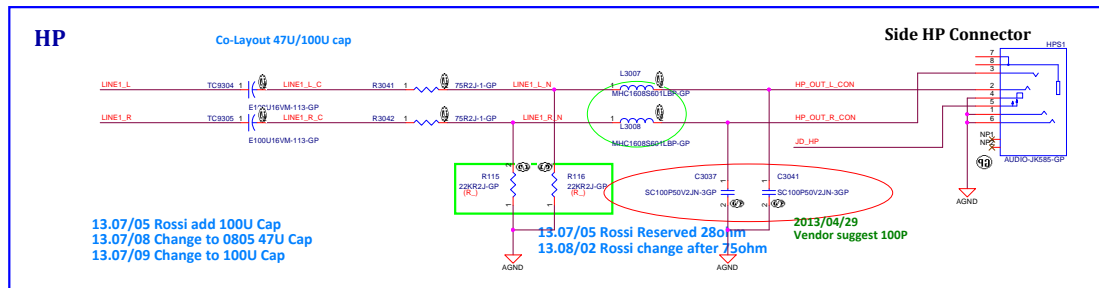
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27 MIC\_VREFL << MIC\_VREFL  
27.28 F\_HPO\_L >> F\_HPO\_L  
27.28 F\_HPO\_R >> F\_HPO\_R  
27 FM\_L\_CODEC << FM\_L\_CODEC  
27 FM\_R\_CODEC << FM\_R\_CODEC  
27 COMBO\_JACK << COMBO\_JACK  
27 MIC2\_VREF0 >> MIC2\_VREF0  
27 JD\_LOT >> JD\_LOT  
27 JD\_HP >> JD\_HP  
27 MIC\_IN\_ID >> MIC\_IN\_ID  
27 MIC2\_R >> MIC2\_R  
27 MIC2\_L >> MIC2\_L  
27 LINE1\_L >> LINE1\_L  
28 FM\_R\_CODEC << FM\_R\_CODEC  
28 FM\_L\_CODEC << FM\_L\_CODEC  
28 LINE1\_L\_N >> LINE1\_L\_N  
28 LINE1\_R\_N >> LINE1\_R\_N



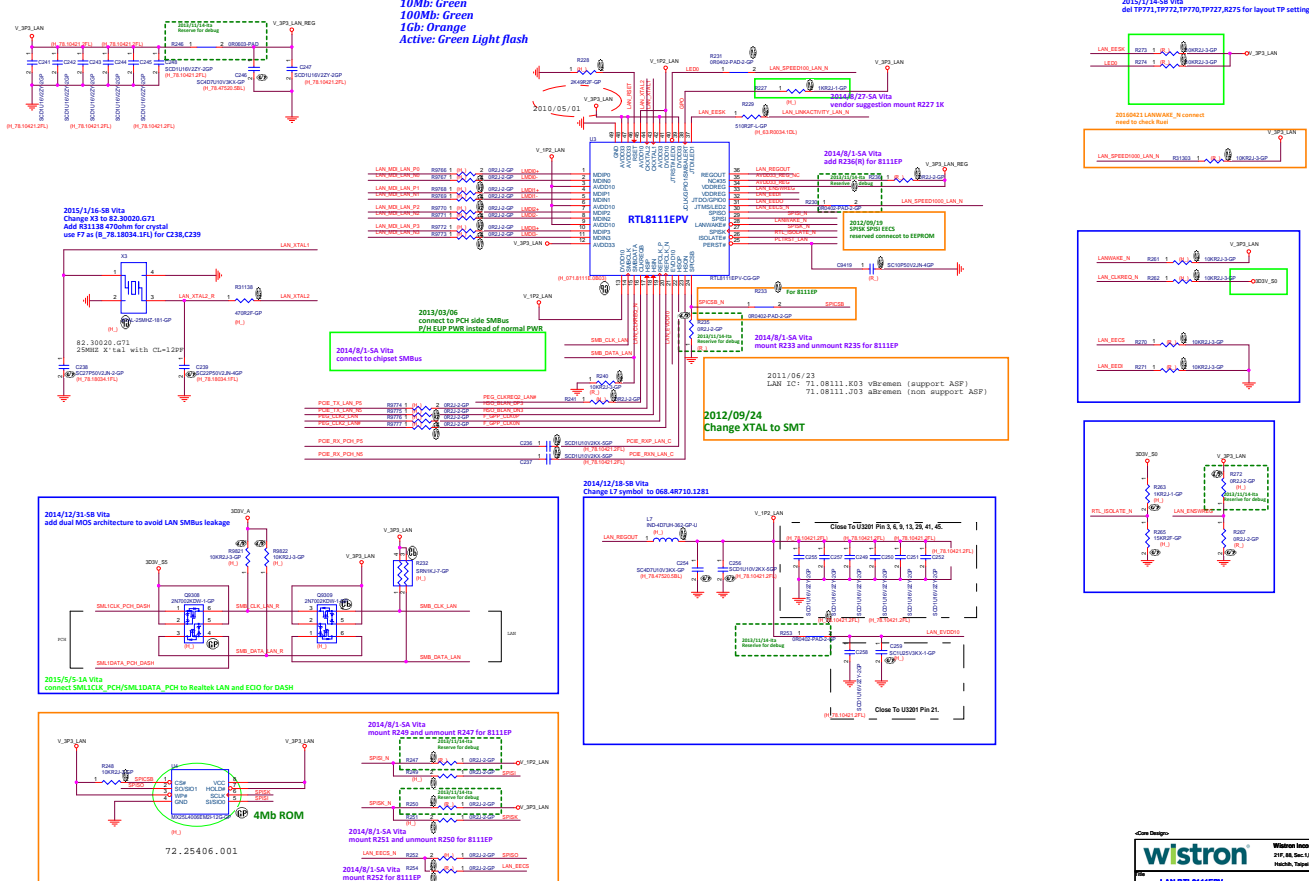
20130910 Ryan



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File Audio IO_Rear_(R)					
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Hsinchu, Taipei Hsin

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Card reader (R\_)

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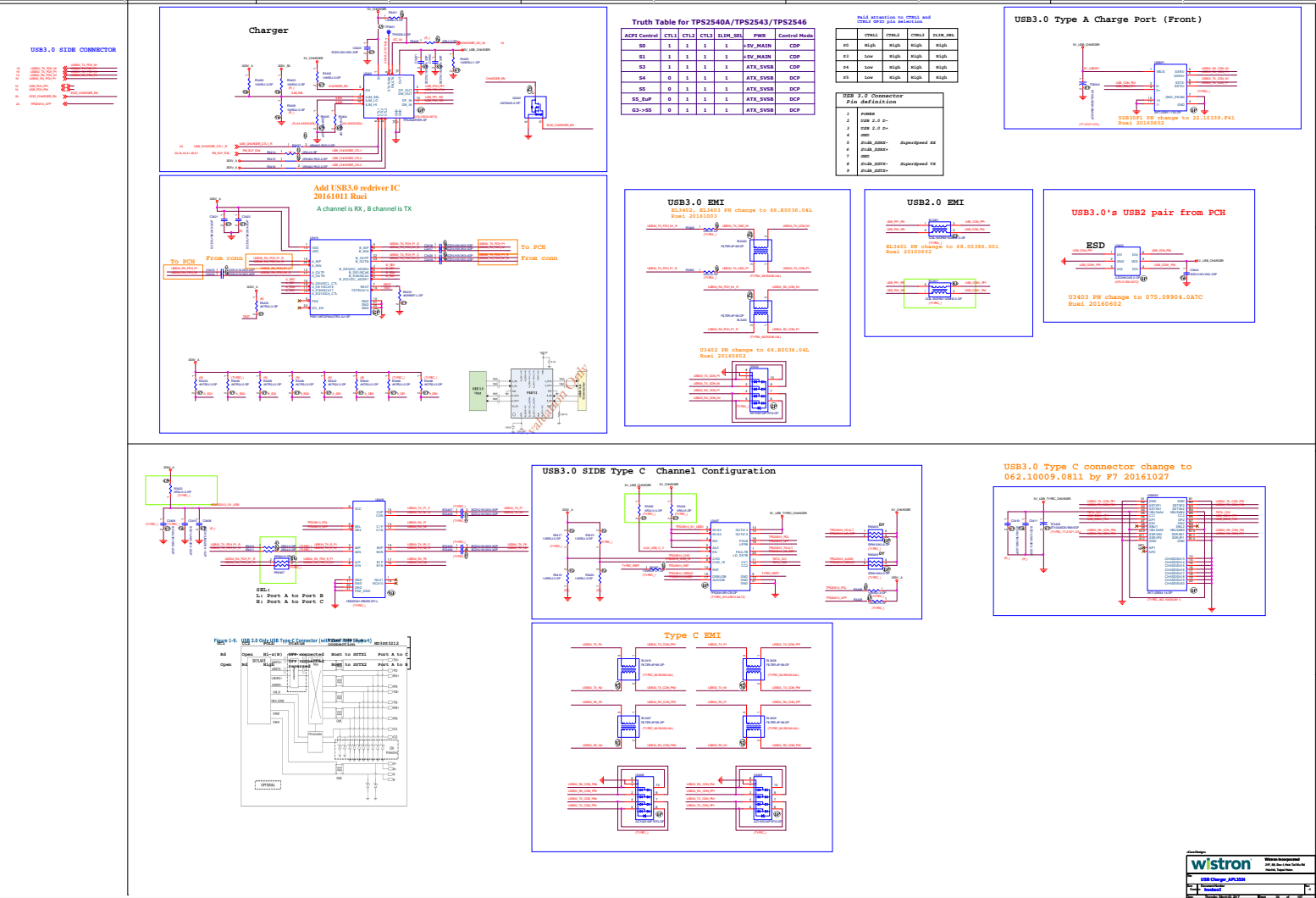
Thursday, March 02, 2017

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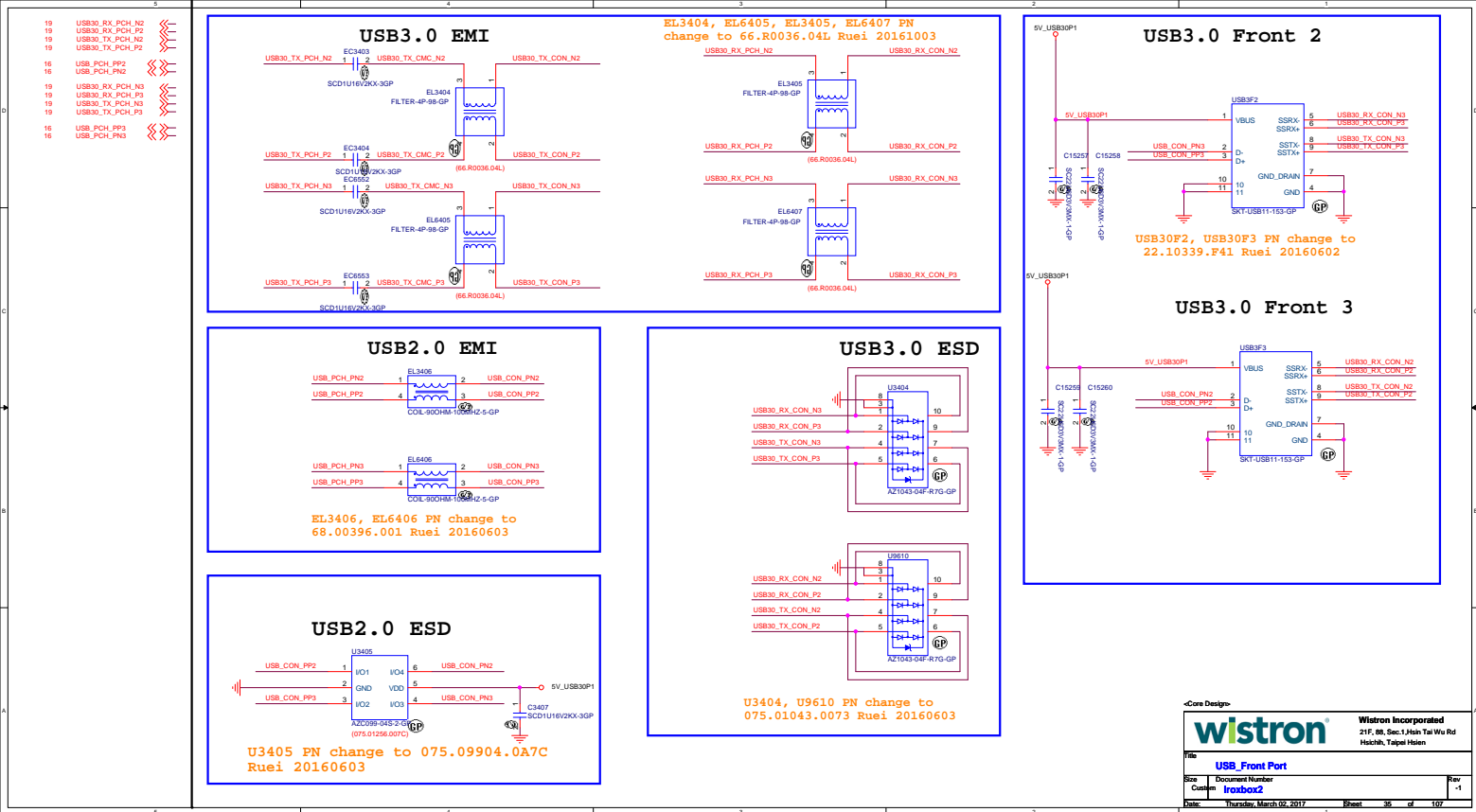
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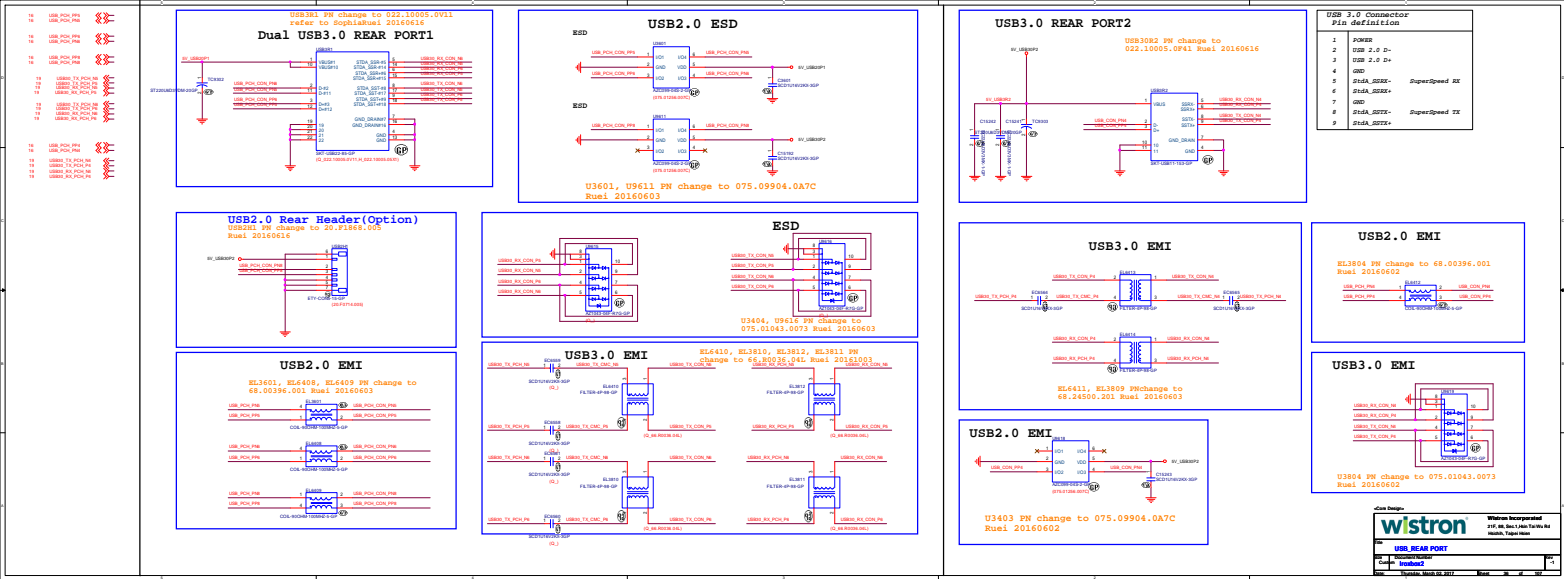
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C	DP InnoBox2	-1	
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File

USB30 (R)

Rev

C

Document Number

iroxbox2

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-1

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of

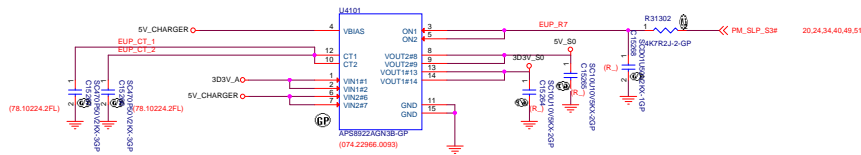
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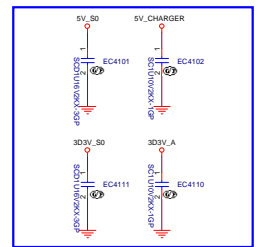
## ANNIE Run Power

5V\_S0 loading  
 $3 \times 5V_{S0} \text{ current of } 2.5'' \text{ HDD} = 3 \times 1A = 3A < 6A \text{ Vout spec}$   
 $3D3V_{S0} \text{ loading} = 1A + 0.5A + 0.025A = 1.525A < 6A \text{ Vout spec}$   
 $2 \times DP = 1A$   
 $4 \times \text{SATA re-driver} = 4 \times 0.125 = 0.5A$   
 Codec 0.025A

Modify 3D3V\_S0/5V\_S0 Logic Control as Load Switch  
 Ruei20160707

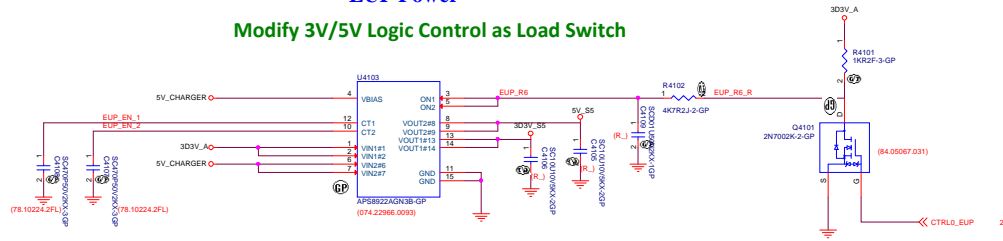


must be closed U4101

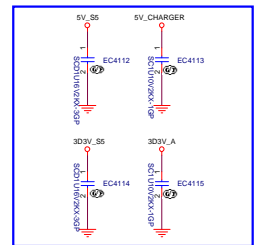


## EUP Power

Modify 3V/5V Logic Control as Load Switch



must be closed U4103



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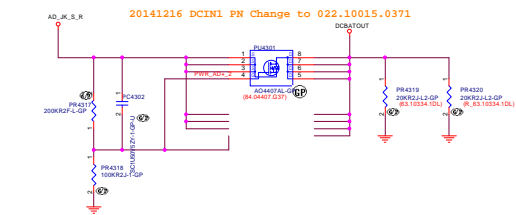
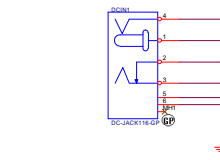
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Doc	Document Number	
Customer	Foxbox2	
Date	Thursday, March 02, 2017	Sheet 41 of 107

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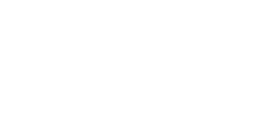
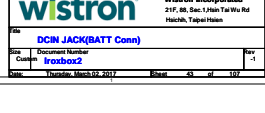
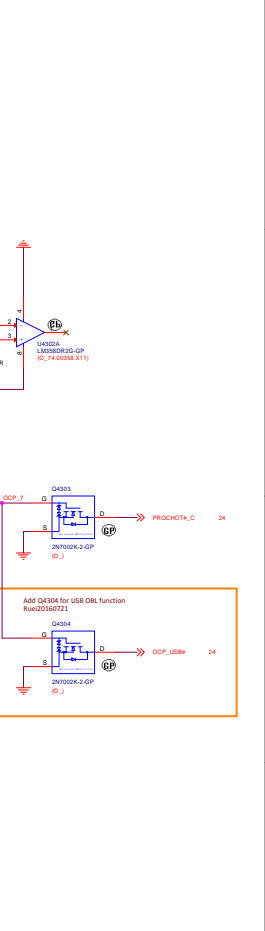
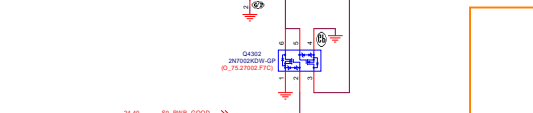
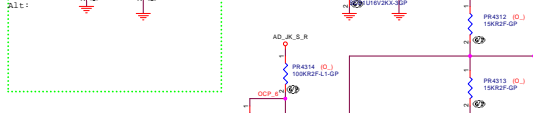
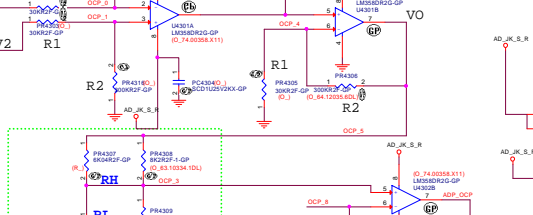
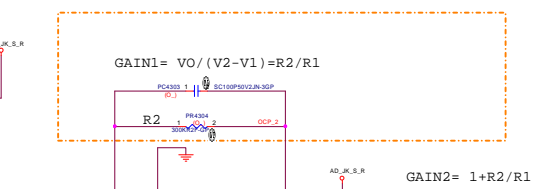
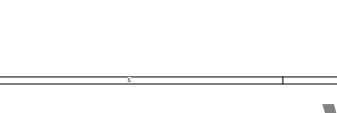
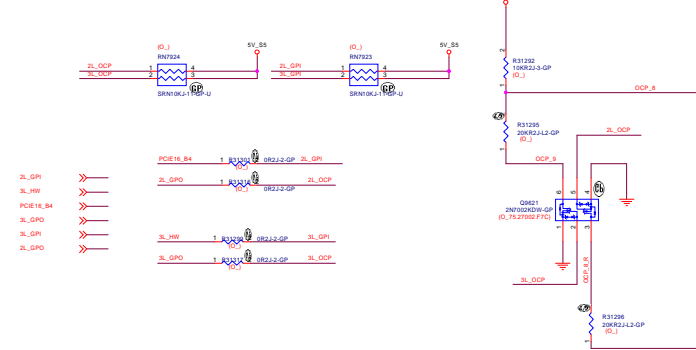


# ANNIE solution

DCIN1 PN change to 22.10037.C61  
Ruei 20160621



	1L	1L+2L	1L+3L	1L+2L	1L+2L+3L	1L+2L+3L
	65W	90W	90W	135W	135W	135W
	MB	VGA card +MB	MB+ extend HDD	VGA card ( R7 ) + MB	VGA card + MB+ extend HDD	VGA card (R7) + MB+ extend HDD
[2L_GPI]	H	L	H	L	L	L
[2L_GPO]	H	L	H	L	L	L
[3L_GPI]	H	H	L	H	L	L
[3L_GPO]	H	H	L	H	L	L



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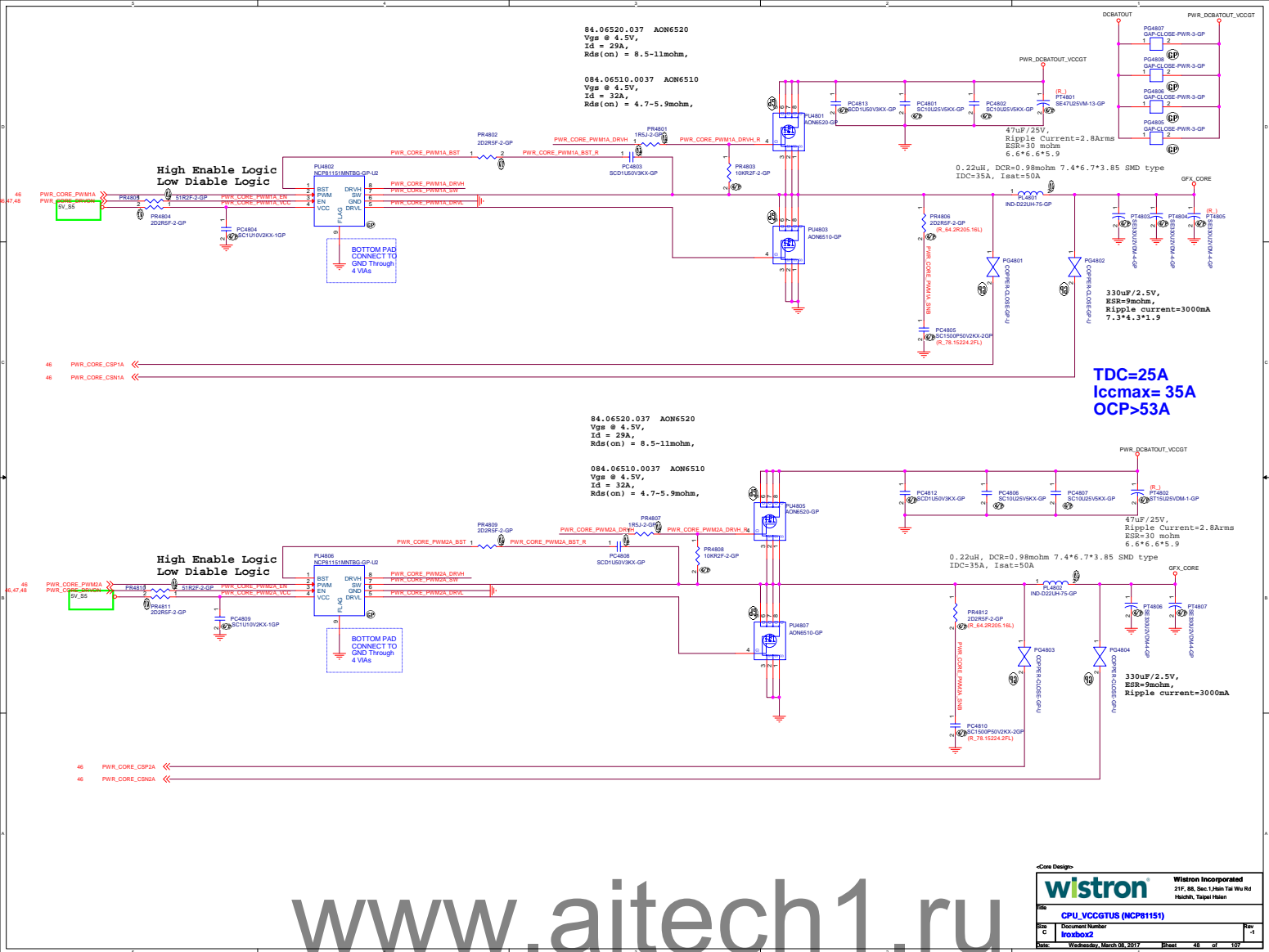
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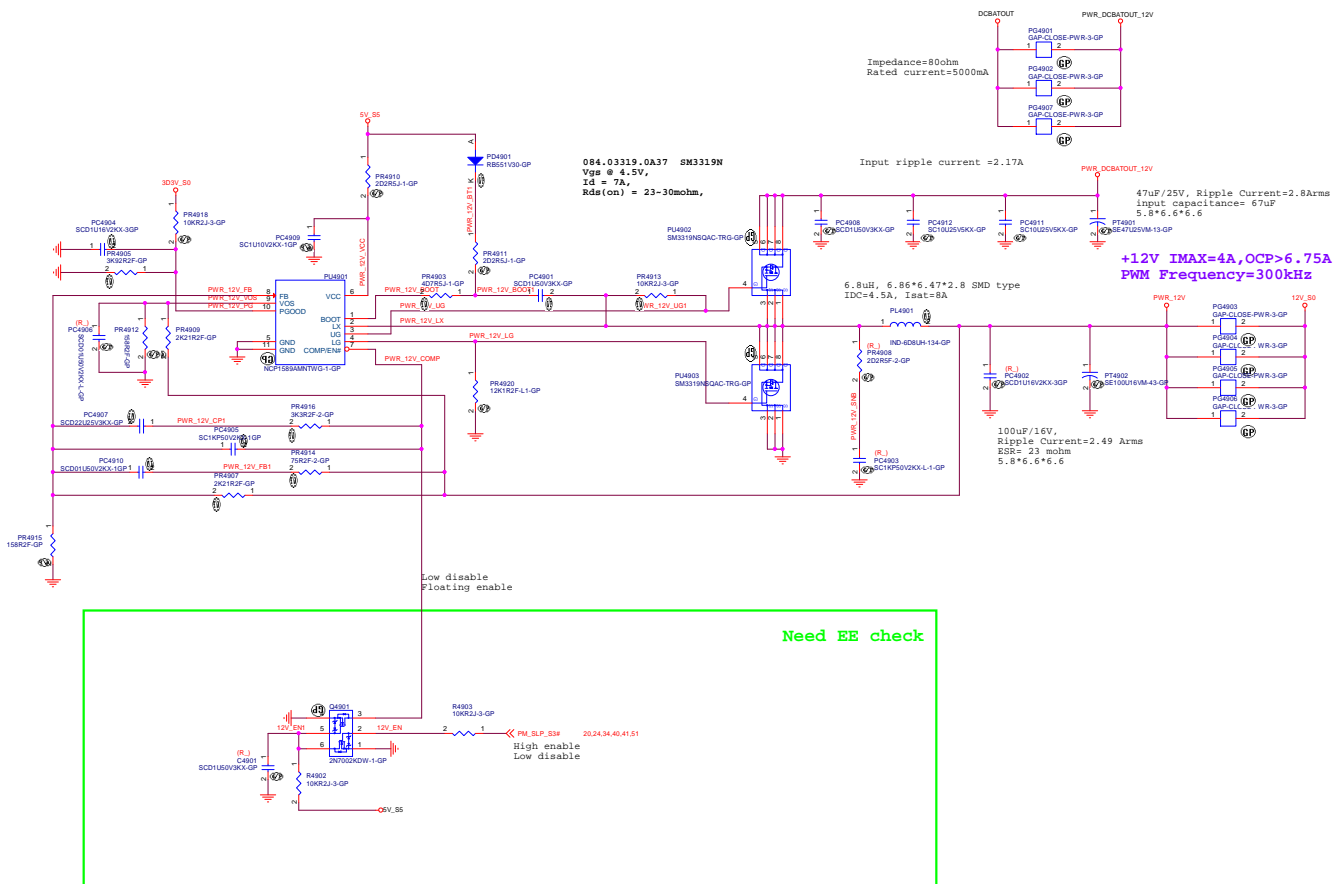




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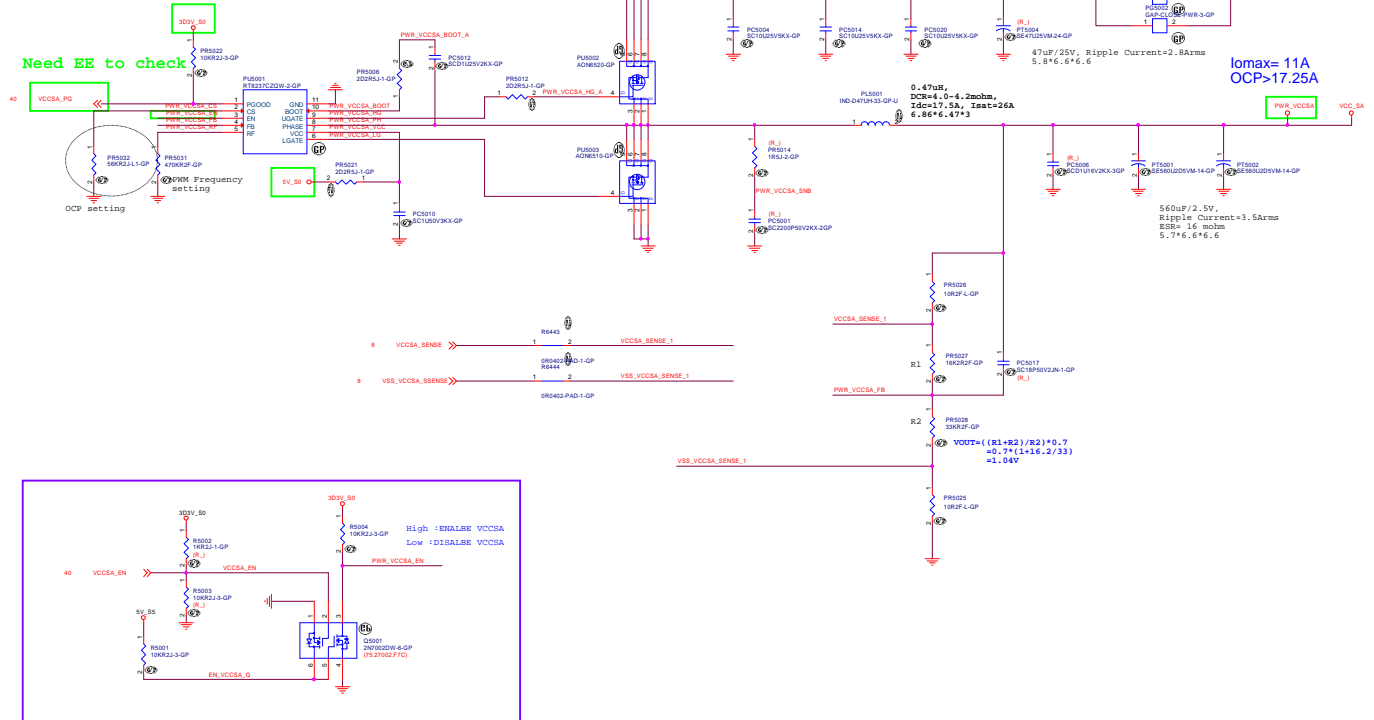


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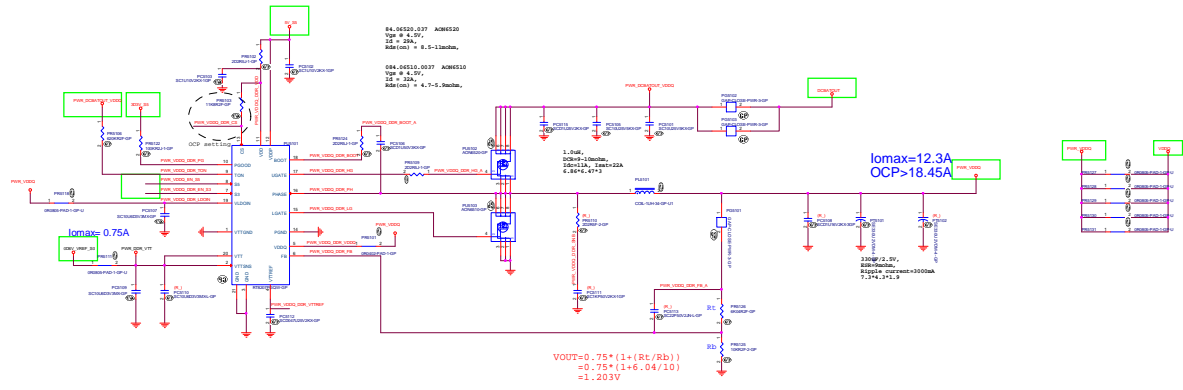
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Rev	C	Document Number	1
broxbox2			
Date		Thursday, March 22, 2017	
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# PWR\_VCCSA

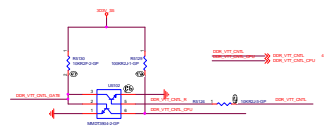
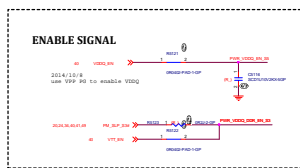
84.06520.037 AON6520  
V<sub>gs</sub> @ 4.5V,  
I<sub>D</sub> = 25A,  
R<sub>ds(on)</sub> = 8.5-11mohm,  
084.06510.0037 AON6510  
V<sub>gs</sub> @ 4.5V,  
I<sub>D</sub> = 32A,  
R<sub>ds(on)</sub> = 4.7-5.9mohm,



## PWR\_VDDQ



## ENABLE SIGNAL



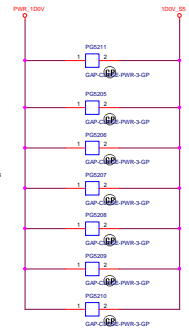
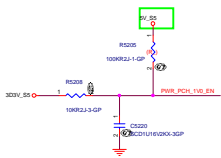
# PWR\_1D0V

Need EE to check

84.06520.037 ACN6520  
Vgs @ 4.5V,  
Id = 29A,  
Rds(on) = 0.5-1.1mohm,  
084.06510.0037 ACN6510  
Vgs @ 4.5V,  
Id = 32A,  
Rds(on) = 4.7-5.9mohm,

Iomax= 7.5A  
OCP>11.25A

## ENABLE SIGNAL



<Crew Design>

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Hsinchu, Taipei, Taiwan

File: PCH\_1D0V (R18237C)

Rev: 1.0  
Crew: 180802

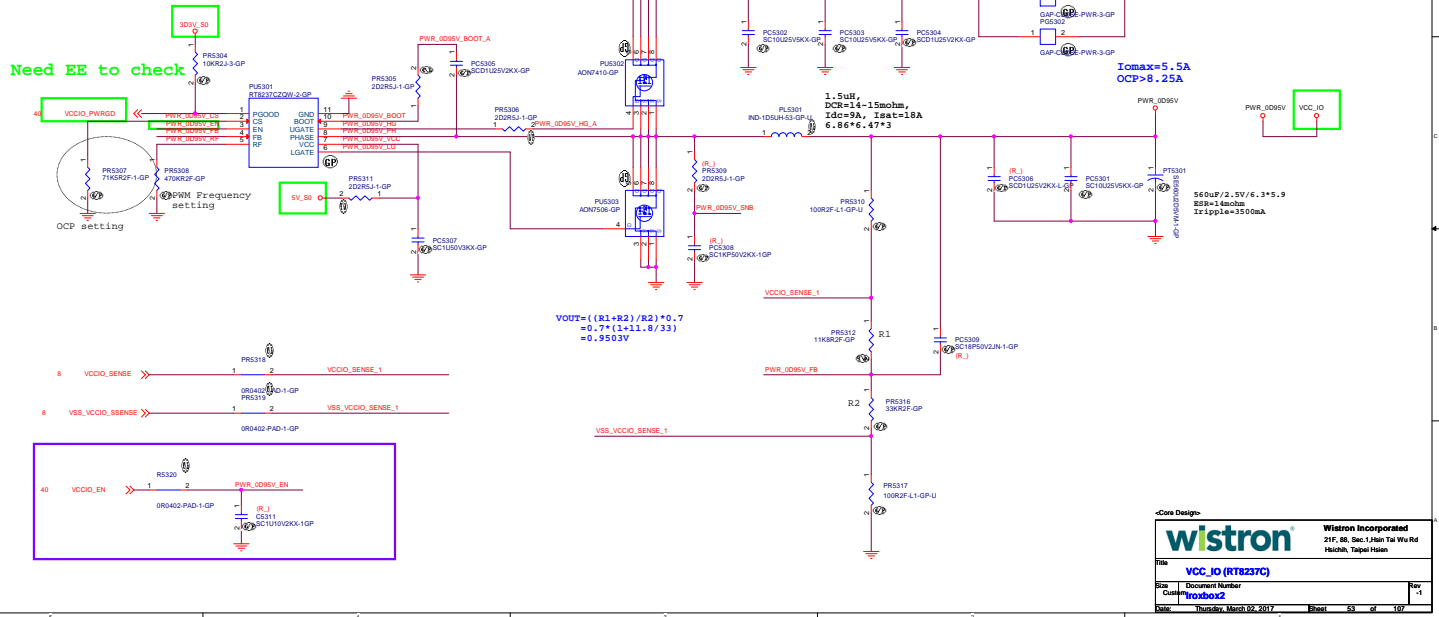
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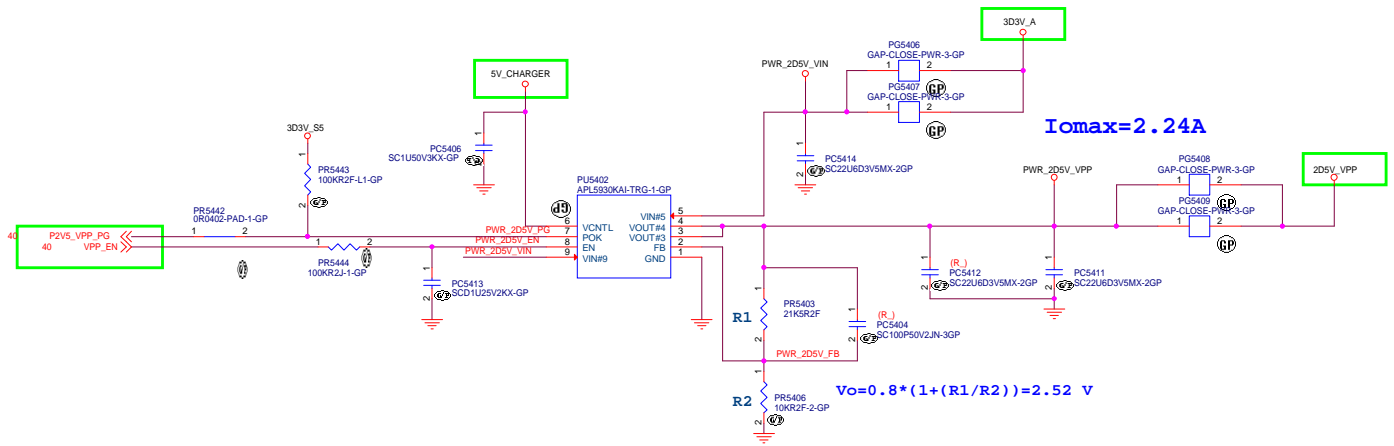
# PWR\_VCCIO

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Vgs @ 4.5V,  
Id = 7A,  
Rds(on) = 24-29mohm,  
  
84.07506.037 AON7506  
Vgs @ 4.5V,  
Id = 3.0A,  
Rds(on) = 13-15.8mohm,



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**PWR\_2D5V\_VPP**



<Core Design>



**Wistron Incorporated**  
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Hsichih, Taipei Hsien

Title	DCDC_2D5V (APL5930)
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Size B	Document Number <b>Iroxbbox2</b>
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Date: Thursday, March 09, 2017

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	Rev -1
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25F, 8th, Sec. 1, Hsin-Fu Rd. No. 10  
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LVDS Connector (R)		Rev
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Date		2014/05/20

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Rev	Document Number	Rev	
C	troxbox2	-1	
Date	Friday, March 03, 2017	Sheet	55 of 107

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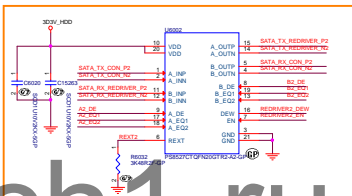
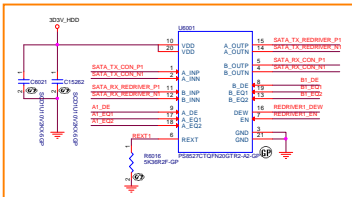
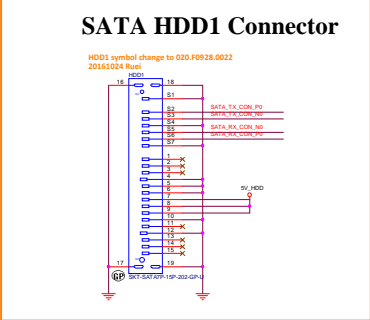
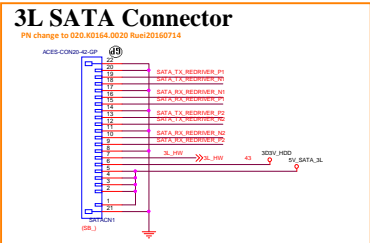
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-Core Design-		Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Hsinchu, Taipei Hsin	
<b>wistron</b>			
File: <b>HDMI OUT (R)</b>			
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EL6001,EL6002 change to 68.24500.201 Ruei 20160614





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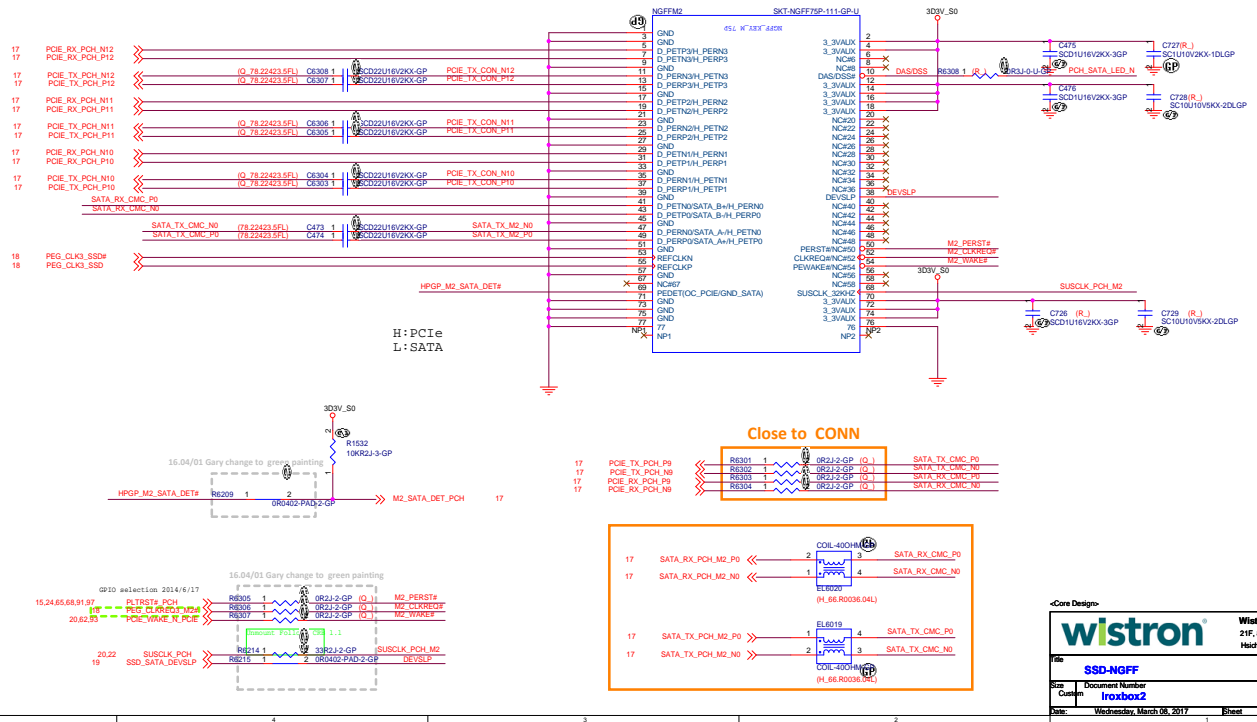
www.aitech1.ru

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<b>wistron</b>			
File: Mini PCIE Card TV Tuner_(R)			
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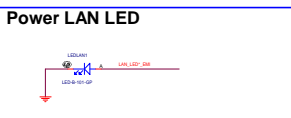
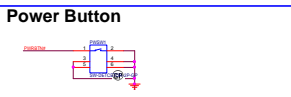
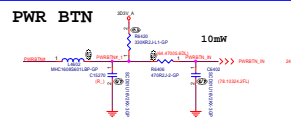
# NGFF(M Key)

NGFFM2 PN change to 062.10003.0731  
Ruei 201611230

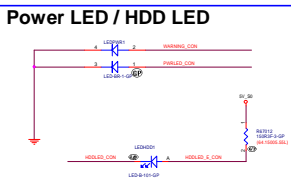


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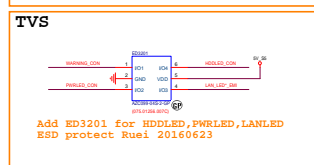
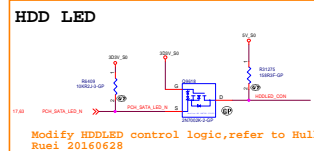
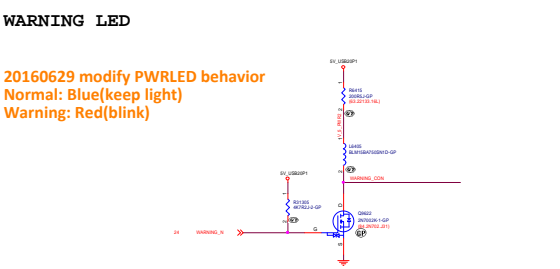
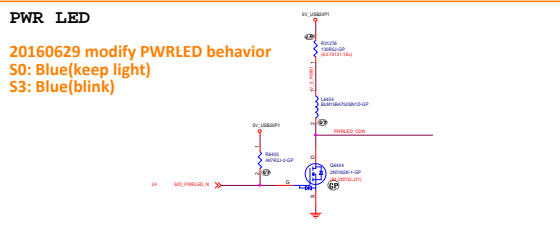
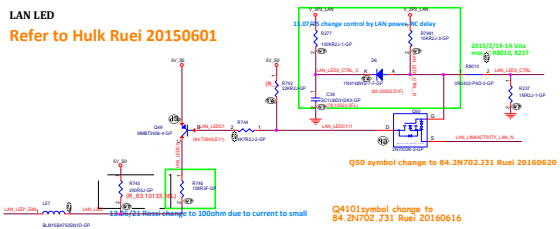
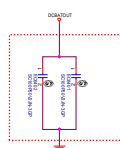
EV\_30 GP LAN\_LANACTIVITY\_LAN\_N  
24 LAN\_LED\_CTRL



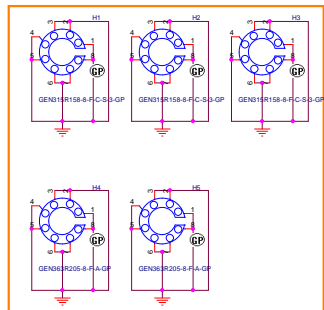
HDDLAN1 change to 83.19217.G70  
Ruei 20160616



LEDPW1 PN change to 83.00195.M70  
HDDLED1 PN change to 83.19217.G70  
Ruei 20160616



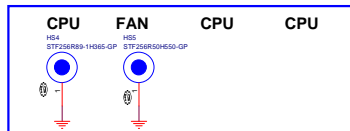
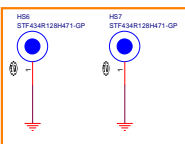
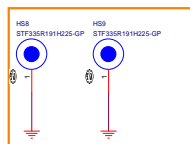
## MB Screw hole



H4,H5 chagne to ZZ.SCREW.551  
20160616 Ruei

SATA Small board stand-off

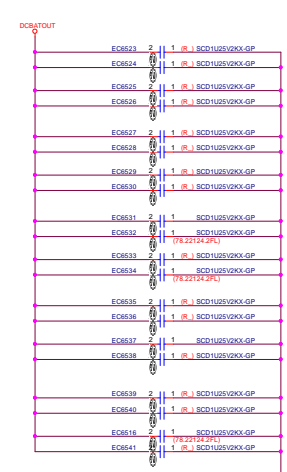
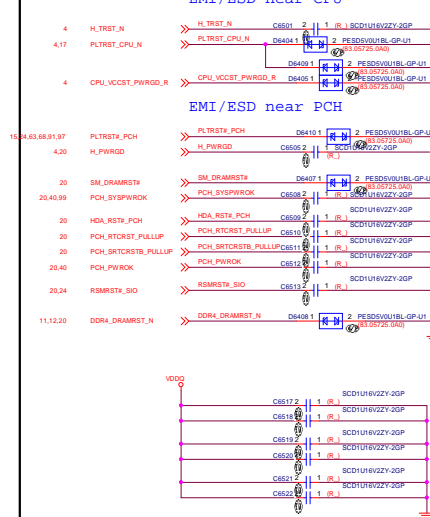
HDD cage stand-off



SATA Small board stand-off PAD  
20160616 Ruei

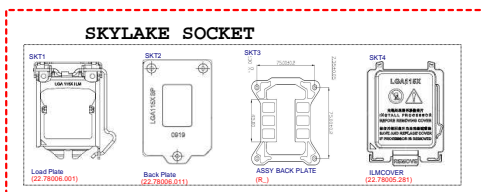


## EMI CAP



## DUMMY BOM

Material part



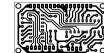
## Battery Symbol

BAT3  
BATTERY CR2032  
(23.20068.001)

Vendor  
P/N:  
23.20068.001  
23.20023.311  
23.22063.001

BAT2  
BATTERY BR3032 30MM  
(R.232420.012)  
Wire Length: 60mm  
耐高溫>85C  
Vendor  
P/N:  
23.21208.061  
23.24220.612

## PCB Symbol



Del PCHHS1 by Thermal--Ryan 0225  
HeatSink Symbol

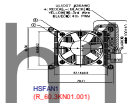


Vendor  
P/N:  
60.3MN01.011(second source)  
60.3MN01.001

## LABEL

LBL1  
LABEL  
(40.38223.011) MB serial NO and MAC address  
LRL6  
LABEL  
(40.38223.011) 35 x 15mm  
LRL6  
LABEL  
(40.38223.011) 45 x 1107.021 -> 70 x 8mm  
LRL6  
LABEL  
(40.38223.011) 40 x 38223.011 -> 30 x 10mm  
LRL6  
LABEL  
(40.38224.001) 40 x 38224.011 -> 30 x 15mm  
CARD  
45.ACA01.0C1 -> 32 x 7mm  
MIC CARD  
345.02801.0001 -> 12 x 6mm

## HeatSink+FAN Symbol



Vendor  
P/N:

-Core Design-  
Wistron Incorporated  
21F, 8B, Sec.1, Hsin Tai Wu Rd  
Hsinchu, Taipei, Taiwan  
File  
Stand off&EMI Cap&DUMMY BOM  
Rev  
C  
Document Number  
Irobox2  
Date  
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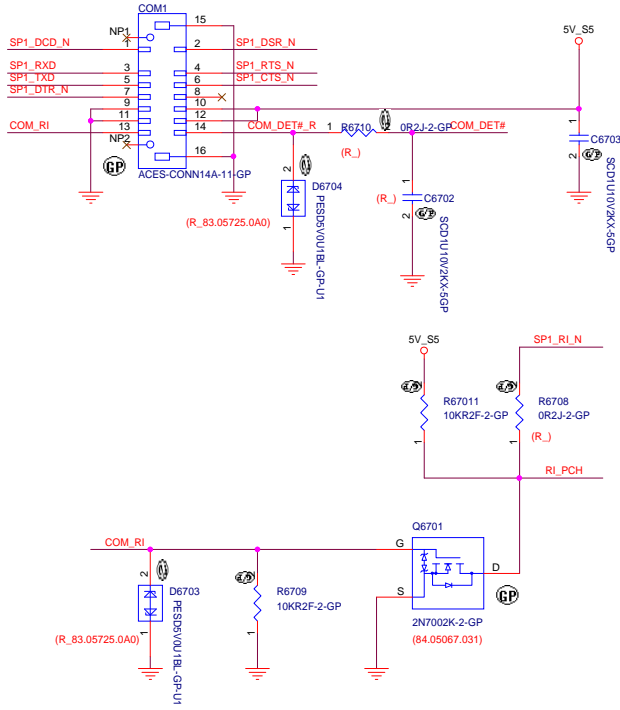
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File		IO Board (R)	
Rev	Document Number	Rev	
C	iroxbox2		-1
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# SPI

24 SP1\_RTS\_N  
24 SP1\_DTR\_N  
24 SP1\_DSR\_N  
24 SP1\_RXD  
24 SP1\_DCD\_N  
24 SP1\_TXD  
24 SP1\_CTS\_N  
24 SP1\_RI\_N  
15 COM\_DET#  
15 RI\_PCH

## SERIAL PORT

20160802 Ruei  
Delete U9609



<Core Design>



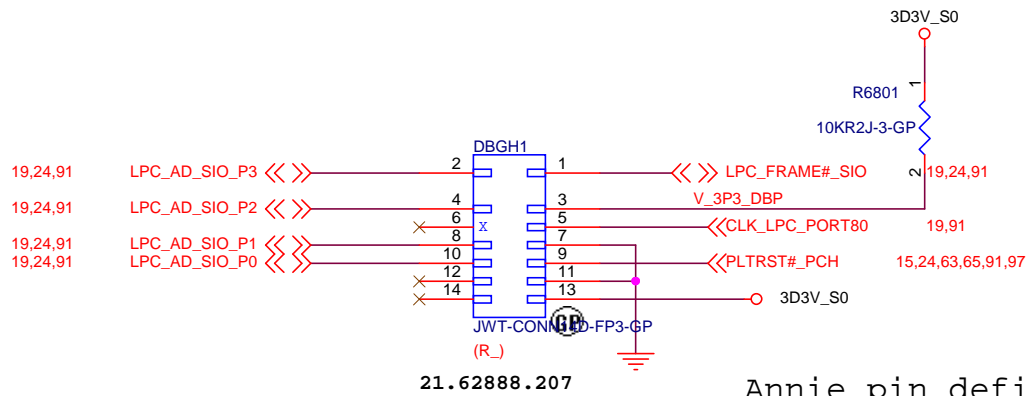
**Wistron Incorporated**  
21F, 88, Sec.1, Hsin Tai Wu Rd  
Hsichih, Taipei Hsien

Title		
COM PORT		
Size	Document Number	Rev
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80 port

Layout close to SIO



<Core Design>

**wistron**

**Wistron Incorporated**  
21F, 88, Sec.1, Hsin Tai Wu Rd  
Hsichih, Taipei Hsien

Title

**Debug**

Size

Document Number

Rev

Custom

**troxbox2**

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LPT_(R)		
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roxbox2		
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-Core Design-		Wistron Incorporated 21F, 88, Sec. 1 Hsin Tai Wu Rd Hsinchu, Taipei Hsin	
<b>wistron</b>			
File: G sensor (R)			
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-Core Design-		Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Hsinchu, Taipei Hsin	
			
File Thunderbolt_R			
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Hsinchu, Taipei Hsin

File

Thunderbolt\_R

Rev

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-Core Design-		Wistron Incorporated 21F, 88, Sec.1 Hsin Tai Wu Rd Hsinchu, Taipei Hsin	
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C	ironbox2	-1	
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Wistron

Wistron Incorporated  
21F, 88, Sec. 1 Hsin Tai Wu Rd  
Hsinchu, Taipei Hsin

File

Thunderbolt\_R

Rev

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-Core Design-		Wistron Incorporated 21F, 88, Sec. 1, Hsin Tai Wu Rd Hsinchu, Taipei Hsin	
File		Thunderbolt_R	
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Wistron Incorporated  
21F, 88, Sec. 1 Hsin Tai Wu Rd  
Hsinchu, Taipei Hsin

File

GPU(I/S) PEG (R)

Rev

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Document Number

iroxbox2

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<Core Design>		Wistron Incorporated	
		21F, 88, Sec.1 Hsin Tai Wu Rd Hsinchu, Taipei Hsien	
File			
GPU(25)DIGITALOUT_R			
Size			
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-Core Design-	
	
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GPU(3S)-VRAM IF_(R)	
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File		GPU Switch	
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-Core Design-		Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Hsinchu, Taipei Hsin	
<b>wistron</b>			
File			
GPU Switch			
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C	iroxbox2	-1	
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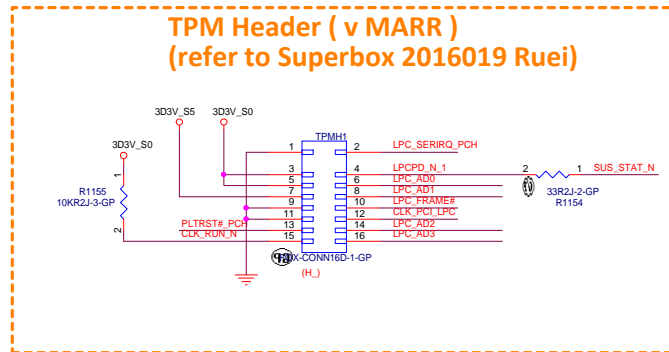
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File		GPU Others	
Rev	Document Number	Rev	
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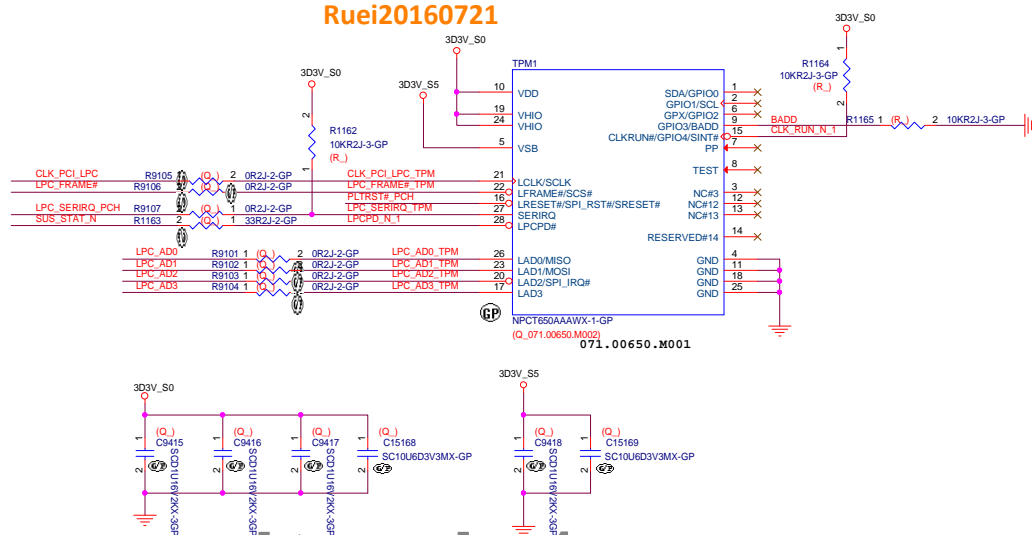
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File		NFC	
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**TPM onboard chip for Q170**  
**change TPM1 symbol to 071.00650.M001(TPM2.0)**  
**Ruei20160721**



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-Core Design-		Wistron Incorporated 21F, 88, Sec.1 Hsin Tai Wu Rd Hsinchu, Taipei Hsin	
<b>wistron</b>			
File			
PS2_(R)			
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File Smart Card (R)			
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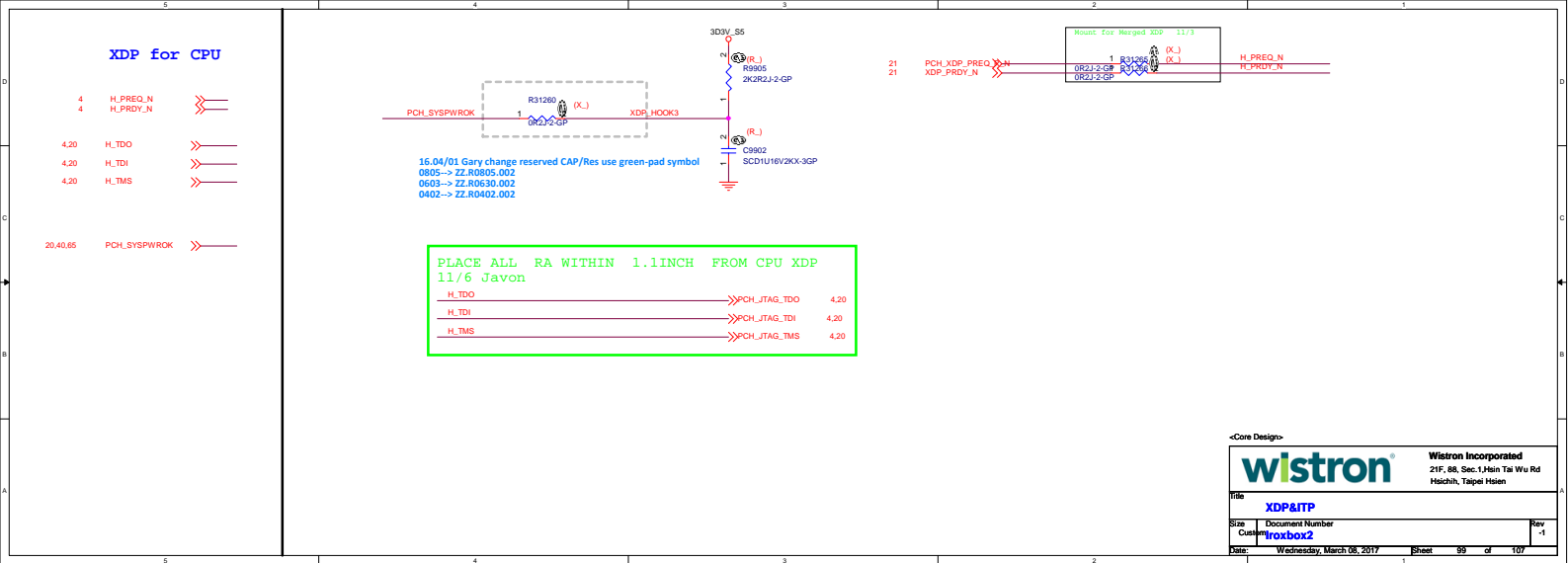
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File LAN Switch (R)			
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-Core Design-		
		
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File		
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21F, 88, Sec. 1, Hsin Tai Wu Rd  
Hsinchu, Taipei Hsin

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## DMI Message

PLTRST#

H\_PWRGD

PWRGD\_3V

PCH\_SYSPWROK

1V\_CPU\_CORR

1V\_Sx

1D35V\_VDDQ\_S3

12V\_S0/5V\_S0/3D3V\_S0

PS\_ON\_N

SLP\_S3\_N

SLP\_S4\_N

SW\_ON\_N

SUSACK\_N

SUS\_WARNB

RSMRST\_SIO\_N

SB5V/SB3V

SLP\_SUSB

PWRBTN\_N

PCH\_SIO\_DPWROK

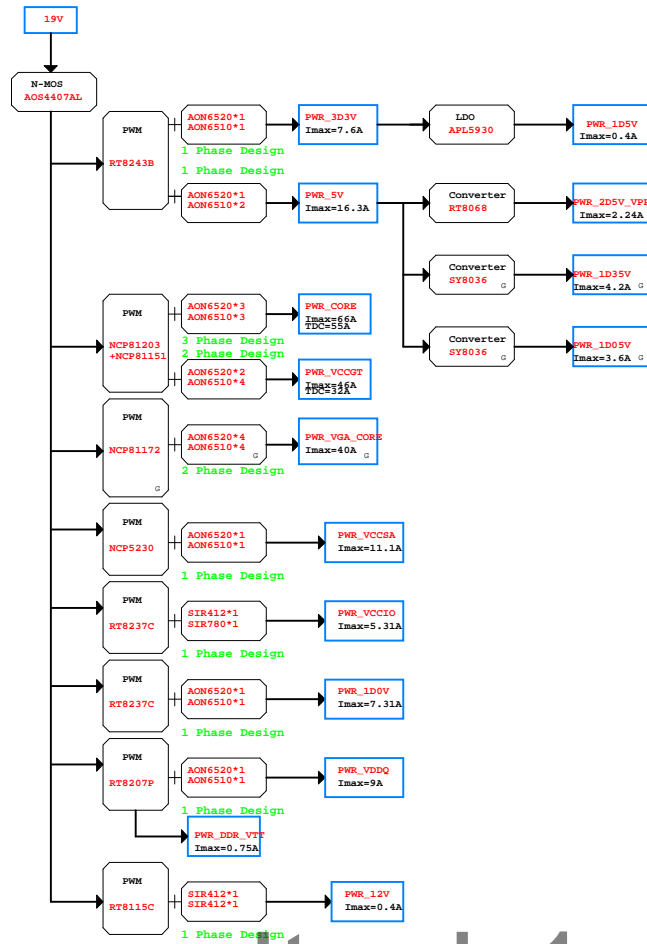
5V\_DS4/ 3D3V\_DS4

RTCCLK

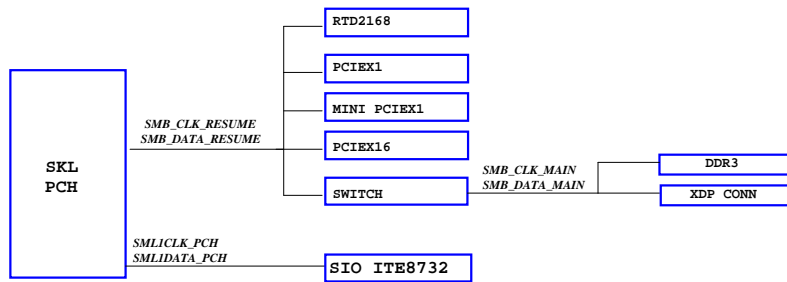
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VccRTC

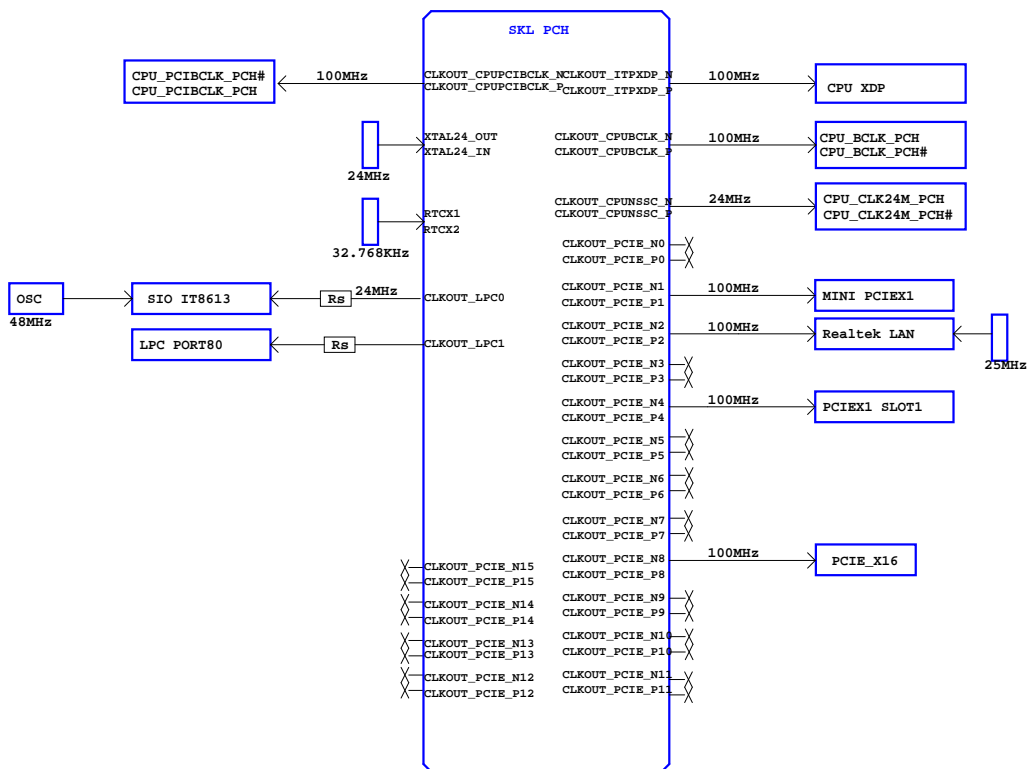
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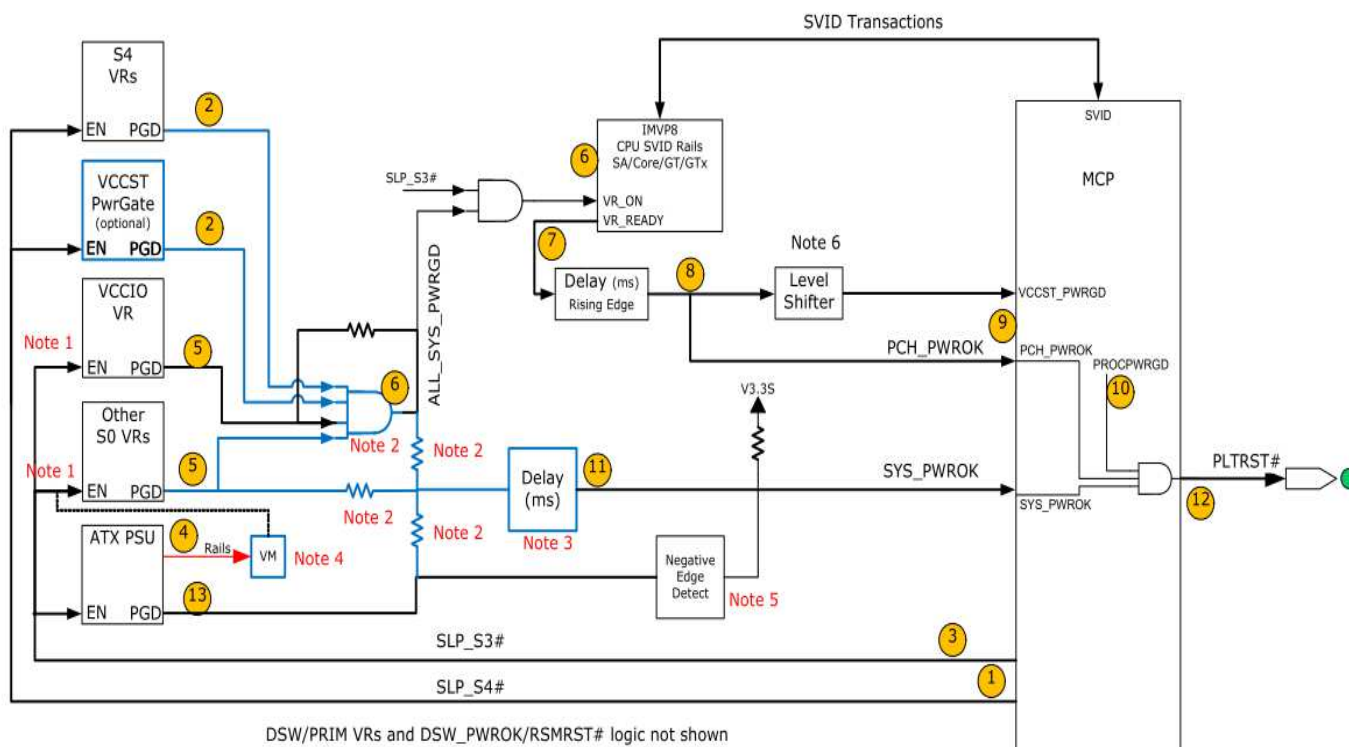
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